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A TWO-DIMENSIONAL MULTIELECTRODE MICROPROBE FOR THE VISUAL CORT--ETC(U)
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(6) A TWO-DIMENSIONAL MULTIELECTRODE MICROPROBE FOR THE VISUAL CORTEX.

(9) Master's THESIS

(14) AFIT/GE/EE/79-37 (10) Joseph Allen Tatman
2Lt USAF

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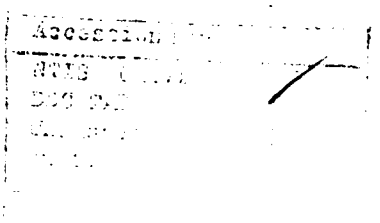
A TWO-DIMENSIONAL MULTIELECTRODE MICROPROBE FOR THE VISUAL CORTEX

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science



by

Joseph A. Tatman
2Lt USAF
Graduate Electrical Engineering
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Preface

In his book of 1966, A Proposed Model for Visual Information Processing in the Human Brain, Dr. Matthew Kabrisky suggested an experiment to test a theory proposed in that book on visual information processing. The search for an array microprobe capable of performing this experiment resulted in the undertaking of this thesis project. The purpose of the device fabricated as part of this thesis was to demonstrate the feasibility of an array microprobe device design proposed by Dr. Borky.

Special thanks are due to Jim Skalski, Russ Scherer, Tom Herbert, Mary Harshbarger, Carol Isbill, Bruce Pecor, and their colleagues at the Avionics Laboratory for their generous support in the fabrication of the microprobe device. The always patient, ever present help of Dr. Borky, the inspiration of Dr. Kabrisky, and the advice of Dr. Wolaver were greatly appreciated. A special thank you to my fiancee, Sharon, for her patience and understanding. And finally, praise to our Creator for making it all possible.

Joseph A. Tatman

Contents

List of Figures

Abstract

The pattern recognition research effort being conducted at the AFIT Bioengineering Laboratory motivated the design of an electrode array microprobe capable of simultaneously recording the bioelectrical signals existing over a large surface area of the cortex of the mammalian brain. Data recorded from this device should increase the present level of knowledge of the interconnections of the various areas of the cerebral cortex and thus be instrumental in the development of theories on the pattern recognition capabilities of the human brain. An implanted system has been designed around this microprobe to detect the cortico-electrical signals, multiplex and modulate these data, and then transmit them across the intact scalp to external recording equipment. The electrode array microprobe, itself, makes use of junction field-effect transistors integrated directly onto the array substrate in order to multiplex the probe's output leads. The first example of a four by four version of the electrode array has been fabricated. It did not function as designed because of technical problems and a revised process schedule was produced.

A TWO-DIMENSIONAL MULTIELECTRODE MICROPROBE FOR THE VISUAL CORTEX

I. Introduction

Background

Significance. This research is significant in that it applies the technology of the integrated circuits industry to the problem of constructing a device capable of simultaneously recording the bioelectrical signals existing over a large surface area of the cortex of the mammalian brain. The analysis of data recorded in this fashion should increase the understanding of how the visual areas of the cortex are interconnected and interact to perform pattern recognition processes. This work was done as part of the pattern recognition research effort being conducted by the Air Force Institute of Technology Bioengineering Laboratory with the goal of building computational electronic systems capable of pattern recognition.

Pattern recognition is the ability of the brain, in particular the human brain, to identify the visual patterns coded by the eye. Pattern recognition processes are very important to those scientists searching for an understanding of the general information processes performed by the brain (Ref 1:219). In their studies of how the different areas of the brain are connected and how intricate neuron interactions function, they most often work with the visual system rather

than the other information processing systems of the brain because of the visual system's greater accessibility for experimentation. It is thought that an understanding of the visual system will significantly contribute to the understanding of the remaining information processing systems of the brain.

Information processing engineers are extremely interested in learning how the human visual system performs pattern recognition because the abilities of their own pattern recognition devices are primitive compared to the capabilities of the biological system. They wish to learn how the biological pattern recognition system works to enable them to build such a system of their own (Ref 2:130).

Present Level of Knowledge. Unfortunately, the pattern recognition capabilities of the human visual system remain a mystery. The ability of the human brain to identify patterns, to analyze the two-dimensional image projected onto the retina and to decide, for example that a particular group of lines is a "4" on the page and nothing else, is almost entirely unexplained. Much is known about the nerve pathways from the retina to the visual cortex, and much about the functioning of the small local units of the cortex; however, how the visual areas of the brain support the mutual interaction of large two-dimensional arrays of elementary functional units, the necessary precondition for pattern recognition, is unknown.

An image projected onto the retina by the ocular optics (Fig. 1-1) is homeomorphically mapped in a topologically accurate fashion through the lateral geniculate bodies onto the primary visual area of the cortex (Ref 2:133). The channels of neurons that perform this mapping are virtually isolated from each other, and thus no significant interaction can take place between them, or thus, between the pieces of the visual image. Therefore, pattern recognition cannot take place along these channels but must occur somewhere in the primary visual cortex or beyond. The primary purpose of these channels appears to be to map the left half of the visual field of each eye onto the right lobe of the visual cortex and to map the right half of the visual field of each eye onto the left lobe of the visual cortex (Ref 2:132).

The processing of the image performed by the primary visual cortex likewise does nothing to correlate between the different pieces of the visual image. The visual areas of the cortex, as well as the other areas of the cortex, are two millimeter thick sheets of neurons divided into integral, independent, functional units of hundreds to thousands of neurons each. These units extend the entire two millimeters through the thickness of the cortex and are between 0.05 and 0.5 millimeters in diameter (Ref 2:133). Computation takes place in these units in the vertical direction, perpendicular to the plane of the cortex. Hubel and Wiesel have extensively researched the processes that these units perform on the image they receive from the retina. They believe

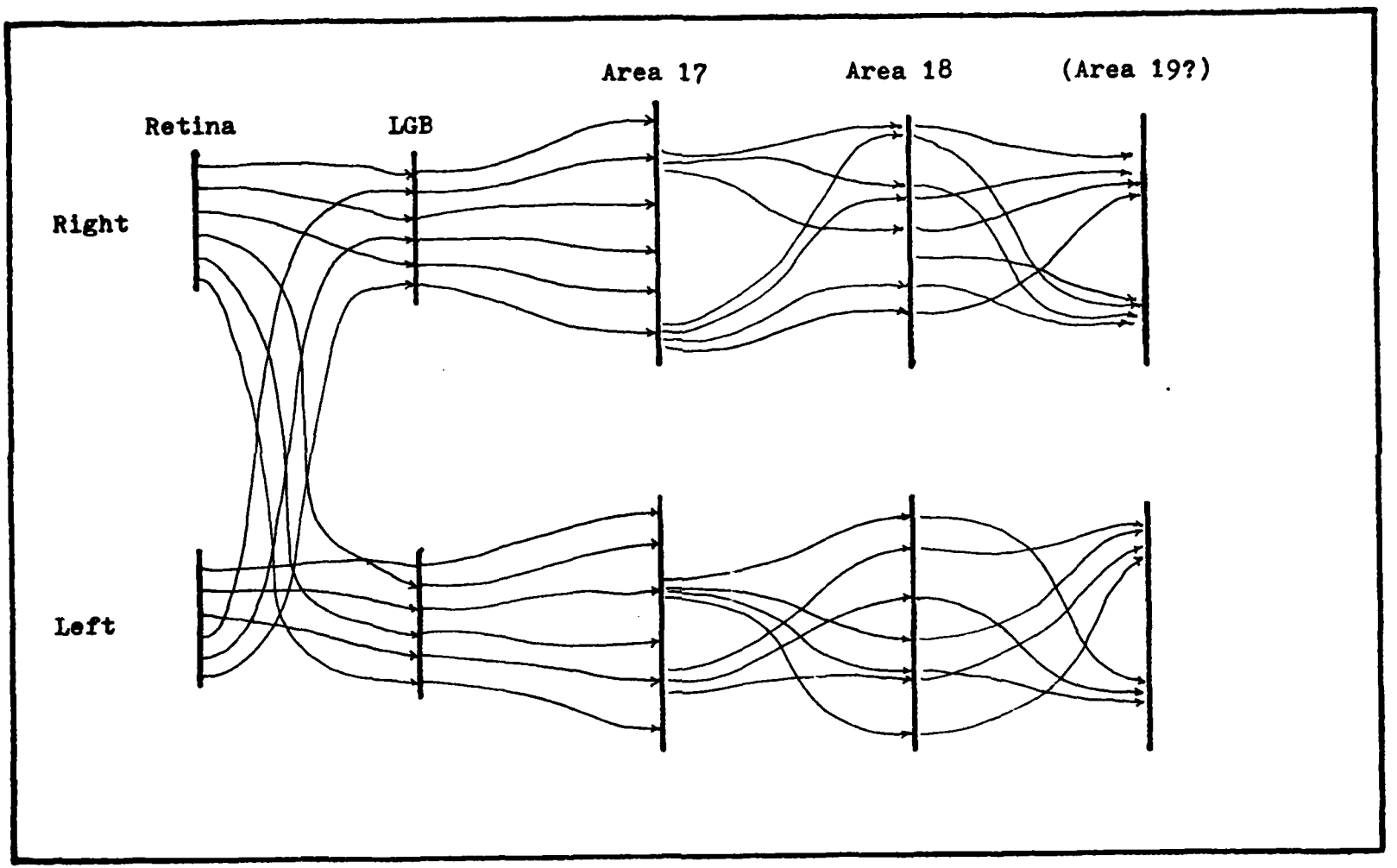

Fig. 1-1. Retino-cortico-cortical connection scheme transmitting visual data from the retinae of the eyes to the visual areas of the cortex, after Kabrisky, et al (Ref 1:134).

that the units' primary purpose appears to be a local analysis of the visual world that enhances the orientations and movements present in the visual image (Ref 3:150-162), but this is by no means certain and there is much controversy as to their actual function.

The data flow laterally across the sheet of the primary visual cortex is therefore nearly nonexistent, and thus there can be no interaction between the different areas of the visual scene where it is first mapped in the cortex. Since all areas of the cortex have this property of no lateral flow of information, the mutual interaction of large two-dimensional arrays necessary for pattern recognition cannot be performed in any single area of the cortex and so must be performed through the interconnections between the different cortical areas (Ref 2:133-134).

In general, very little is known about the anatomy or the function of the interconnections between the different areas of the cortex, including those that are known to process visual data. It is known, however, that several distinct areas of the cortex process visual data. It is also known that the interconnections between these areas are very dense and seemingly random (Fig. 1-1). This sort of organization has been shown to be theor e tically capable of supporting the type of mutual interaction of large two-dimensional arrays necessary for pattern recognition (Ref 2:134).

One branch of contemporary brain research in the area of pattern recognition is directed along the lines of searching for the ways in which the elementary functional units of the brain interact to perform the complex neural functions necessary for pattern recognition.

Neuroanatomists and neurophysiologists both contribute to the solving of this problem. The anatomists attempt to discover the three-dimensional distribution of neurons in the cortex and the ways in which these neurons are connected through chemical means. They stain the nerve cells to trace their axons from the cell body to their terminations onto other neurons.

Neurophysiologists, on the other hand, attempt to discover the pattern recognition processes of the brain by studying the responses of different areas of the brain to visual stimuli by recording the electrical signals of the cortex with electrodes. The advances in recent years in the use of integrated circuit technology to build better electrodes, and most importantly, well controlled electrode arrays, has greatly increased the abilities of neurophysiologists to study brain responses to stimuli.

Neurophysiologists have begun to use the standard photolithographic techniques of the integrated circuit industry to build arrays of metal microelectrodes onto silicon or glass substrates. One such microprobe has eight electrodes on a glass substrate arranged on 0.3 millimeter centers and each having a diameter of 0.05 millimeters (Ref 4:421).

Devices such as these have been successfully used in studies of the auditory nerve (Ref 5:494-500) and studies of cortical electrical activity during seizures (Ref 6:414).

Since silicon is the standard substrate of the integrated circuit industry, and since it is often possible to use silicon as the substrate in the above microprobes, it is also possible to integrate active devices such as amplifiers directly onto the substrate that is supporting the electrodes (Ref 7:212-219). Also, a system of complicated silicon integrated circuits to stimulate the electrodes of an auditory prosthesis has been built that is capable of being chronically implanted under the scalp and receiving information and power through ultrasonic and RF links, respectively, across the intact skin (Ref 8). Combining these two ideas, it is conceivable to build a chronically implantable electrode array microprobe with signal processing circuitry integrated directly onto the electrode carrier substrate. This system could record cortical electrical signals, process and modulate them, and transmit this data outside the body across the intact skin.

In summary, though much is known about individual neurons and interactions of small groups of neurons, very little is known about the mutual interaction of large two-dimensional arrays of neurons that must take place for pattern recognition to occur. It is known however, (from the anatomy and physiology of the retinal-cortex channel and of the areas of the cortex) that the processes necessary for pattern recognition must take place in the interconnections

between the different cortical visual areas. Recent advances in the use of integrated circuit techniques for microelectrode fabrication gives neurophysiologists a valuable new tool for studying these cortico-cortical interconnections.

Problem

As reported in the background, it has been shown that the dense and apparently random interconnections between visual areas of the cortex could support one type of computation that would enable the brain to perform pattern recognition. Kabrisky has proposed a theory that these interconnections perform a Fourier transform computation as one of the major sub-tasks in the pattern recognition process (Ref 2:134-135).

In order to test this theory it is necessary to carefully analyze large amounts of data simultaneously recorded from an array of closely spaced electrodes on centers of the order of 0.05 to 0.5 millimeters in several of the related visual areas of the cortex (Ref 2:135). This thesis project addresses the problem of constructing a system using integrated circuit technology to perform this simultaneous recording of cortical potentials.

Toward this end, there are two goals of this research. The first is to design a system capable of testing Kabrisky's theory in order to study the feasibility of actually carrying out the design and building of such a system. The second goal of this research is to design, build, and test a novel integrated circuit multiplexed matrix electrode array which

would be an integral part of the above system. This circuit would make feasible the idea of simultaneously recording from a huge array of electrodes to gather the necessary data to test the theory.

Scope

In order to keep the first system design reasonably simple, the problem is limited to a system containing an electrode array of a few thousand electrodes and a six-bit data channel to allow the data to be stored on random access memory through the use of a microcomputer in real time. The design was carried to the point of a simplified circuit diagram of a possible implementation of the system. This circuit design reflects the feasibility of such a system. It is expected that improvements will be made in design during the actual building of the system.

The multiplexed matrix electrode array to be fabricated will be initially limited to a four by four array of electrode-transistor cells. This device will be sufficient to adequately test the multiplexed electrode array idea, while keeping the fabrication process from becoming too difficult.

Approach

The approach taken in the system design portion of this work was to do a detailed study of the requirements of such a system, to develop from these a system block diagram design with the detailed functional requirements for each block, then to propose one possible circuit implementation of the

block diagram design and to discuss the capabilities of that implementation based on present-day technology.

In the electrode fabrication portion of the thesis project the approach was to design such an electrode, build the electrode using standard integrated circuit techniques, and then do a functional test of the device. A physiological in vivo testing of the device will be part of a later thesis.

Sequence of Presentation

The Fourier transform pattern recognition theory of Kabrisky, which stimulated the need for this thesis, will first be discussed along with an analysis of the problem posed by attempting to test this theory. This will be followed by a description of the system designed to test the theory. Shifting emphasis, the design and fabrication of the four by four multiplexed electrode array will be described and then the electrode testing methods and results discussed. Ending the report will be a discussion of the overall research effort and finally the conclusions and recommendations for further study arrived at through the research effort of this thesis.

Summary of Results

Through a system design exercise it has been determined that it is feasible to build an implantable electrode array system to record data from the cerebral cortex and to transmit this data to outside the body transcutaneously. It is expected that this system could contain an array of

one hundred by one hundred electrodes, scan this array one hundred times per second, transmit the recorded data at a rate of one million words per second, and consume approximately ten milliwatts power.

A prototype four by four multiplexed electrode array was designed and the mask set generated for its fabrication. A trial run through the process schedule resulted in a non-functional device. However, the revised process schedule arrived at through this trial run is expected to yield working devices.

II. Problem Analysis and Theory

Theory (Ref 2)

As stated in the background section of this thesis, the manner in which the brain processes visual information in order to do pattern recognition remains a mystery. It is known, however, that the retinal image is homeomorphically mapped onto the primary visual cortex and from there mapped onto several other related areas of the cortex. Because of the anatomical and physiological structure of the cortex, any processing performed on these maps by the different visual cortical areas is highly localized. Any individual area of the cortex performs no computation on its map of the visual image as a whole, but rather performs computation only over small local areas of the map. Therefore, the necessary interaction of the elements of the visual map, a two-dimensional array, must be met by the interconnections between the various visual areas of the cortex as the visual information is transmitted between the areas.

Unfortunately, very little is known about the systems and methods of data transmission between the different areas of the cortical sheet. It is known, however, that the data of the primary visual cortex is broadcast wide and seemingly randomly to the successive visual cortical areas. Kabrisky has proposed a theory on the type of pattern recognition computation that this wide and random broadcast of data between the cortical areas could support. His theory will be discussed

next, then the problem of designing the system necessary to test the theory will be stated. Finally, the system proposed in this thesis to test Kabrisky's theory will be introduced and the specific requirements of that system listed.

The optical computer is one example of a system that performs computation through spatially dispersive broadcasts of data between the various elements of the system. It does this through the interference and reinforcement of the sinusoidal electromagnetic fields of a group of light rays as they pass through a transparency then through a system of lenses. The reinforcement and interference is performed by the lenses as they alter the path lengths of the lines of the electromagnetic field passing through them. The resulting change in propagation times of the electromagnetic waves, as a function of their point of origin in the image, results in the reinforcement and interference of the electromagnetic waves necessary for computations to occur. One of the interesting computations that such an optical computer can perform is the two-dimensional Fourier transform of a phototransparency.

Discrete systems, specifically optical fiber systems and digital computers, can be designed or programmed to approximate the computational ability of the optical computer. The systems control the propagation of information along discrete pathways to perform the reinforcement and interference and thus perform the same sort of computation as the optical computer.

Kabrisk's theory states that the passing of information between the different visual areas of the cortex could also approximate the Fourier Transform computation performed by optical computers. The axons of neurons, which perform the mapping function of one cortical area onto another, would be analogous to the discrete information pathways of the above systems. The axons transfer information to a cortical area by either depolarizing or hyperpolarizing the membrane potential of the postsynaptic neuron. This change in membrane potential is known as an excitatory postsynaptic potential (EPSP) in the depolarizing case, or as an inhibitory postsynaptic potential (IPSP) in the hyperpolarizing case. These EPSP's and IPSP's would perform the interference and reinforcement function of the above systems. In order for the cortex to support this sort of computation, it is necessary that the cortico-cortical communication system be capable of maintaining consistent relative propagation times and that it provide overall synchronization of activity.

The purpose of this thesis is to investigate the feasibility of designing a system capable of recording the data from the cortical areas necessary to discover if the above timing requirements are met by the cortico-cortical data transmission system of the brain.

Problem Analysis

To test the cortex for its fulfillment of these timing requirements requires careful analysis of vast amounts of

data from an electrode system which records the cortical signals existing across large areas of related cortical areas which deal with vision (Ref 2:135). This system must simultaneously record from a large two-dimensional array of electrodes extending over a significant portion of the appropriate cortical surfaces. The signal recorded by an individual electrode of this system will be a sinusoidal summation of the membrane potentials of the neurons lying near the surface of the electrode. There are approximately 10^5 neurons per millimeter squared across the surface of the cortex. It is thought that the interelectrode spacing of the array of the proposed system should be on the order of 0.05 to 0.5 millimeters, the estimated diameter of the independent computational units of the cortex, to yield sufficient data (Ref 2:135). The system should be chronically implantable to make it possible to record large amounts of data over extended periods of time under varying conditions. The system should digitally store the recorded data external to the experimental subject to facilitate analysis.

DeMott has experimented with a system designed along these lines (Ref 9). His electrode array contained 400 electrodes on 0.25 millimeter centers. The probe itself consisted of a bundle of 400 insulated wires, the ends of which, with the aid of a plastic filler, formed a flat electrode array surface which rested on the cortical surface during recording. The wires led to 400 amplifiers which formed the input stage of the recording system.

This system is not suitable for our purposes. The bundle of wires approach is bulky and awkward and would be nearly impossible to chronically implant. Resolving the crosstalk problem among the bundle of output leads would be difficult. Finally, with one output lead for each electrode, the system does not lend itself to being extended to the thousands of electrodes needed for our purposes.

Advances in recent years in semiconductor technology make possible the design of an integrated circuit device capable of recording a large array of bioelectrical signals over the cortical surface through the use of a multiplexed matrix array of electrodes. Matrix multiplexing the array immediately reduces the number of output leads to one lead per column of electrodes rather than one lead per electrode. Further circuitry could be integrated directly onto the same substrate that supports the electrode array to further multiplex the column leads down to a single data output channel. This same circuitry, together with a separate tunnel diode transmitter, could transmit the data on this one channel through the intact scalp to a data receiving and storage system external to the subject. Through the microscopic dimensions possible with integrated circuit technology, the physical size of this electrode-transmission system can be kept very small to enable it to be chronically implantable. This same miniaturization, combined with the reduction in the crosstalk problem due to the multiplexing of output leads, enables the device to be extendable to thousands of electrodes. The system design requirements of such a device

are listed in the following paragraphs.

System Requirements

Objectives.

1) Simultaneously record the bioelectrical signals existing across as large an area as possible of the visual areas of the cortex, multiplex this data onto a single transmission line, and transmit it to outside the test subject.

2) Be biocompatible, suitable for long-term implantation.

3) Require low voltage and low power consumption.

4) Permit transcutaneous transfer of power and information between the internal and external subsystems.

5) The electrode substrate must fit between the skull and cortex and the transmitter and power circuitry fit between the skull and scalp without damaging the tissue.

6) Exhibit long-term reliability.

Specific Requirements. Functionally, the implanted system must simultaneously record biopotentials from the electrodes of the array compared to a ground plane around the array. The system must time multiplex these signals onto a single data channel, encode the data on that channel to six-bit precision, and then transmit the data to outside the animal. The entire array must be scanned at a frequency of 100 times per second to provide an accurate picture of the sinusoidal bioelectrical signals which have a maximum frequency of approximately forty Hertz. The system must preserve the accuracy of the signals by minimizing crosstalk

among the output leads and by minimizing both the electronics noise and the neural noise from active nerve cells lying adjacent to the circuitry. The system must also transmit a synchronization signal to coordinate the internal and external systems.

The system must record from as large an area of the cortical surface as possible with as many electrodes as possible with an interelectrode spacing of between 0.5 and 0.05 millimeters. This spacing is suggested by the theoretical diameters of the independent functional units of the cortex (Ref 2:135). Further research must determine a sufficient, minimal interelectrode spacing.

For the implanted device to be biocompatible in the subdural space, the device should not affect the functioning of the cortex tissue. Nor should the device electronics be adversely affected by being submersed in the cerebrospinal fluid (CSF) over an indefinite period of time. To not damage the tissue over the long-term, the probe must be noninvasive, that is, the probe must measure the cortical potentials extracellularly. Also, there must be no net charge transfer between the electrode surface and the electrolytic CSF. The electrode must therefore be capacitively coupled to the tissue. This requirement is met automatically by the capacitive nature of the electrolyte-electrode interface. To minimize shock hazards, the supply voltage to the implant should be kept to a minimum and be well insulated from the tissue.

The implant must be chemically inert in the cerebrospinal fluid environment. The device's presence in the CSF must not produce corrosive or toxic by-products.

To enable the device to be long-term implantable without degradation of its performance, it is necessary to guard against two principle failure modes (Ref 10:281). First, water vapor must not be allowed to accumulate on the surface of the integrated circuit. This vapor forms conducting bridges which can short together components of the circuit. The second major failure mode is poisoning of the integrated circuit surface by the ions of the CSF. This will in general degrade the performance of the integrated electronics by increasing the reverse bias current of p-n junctions. To guard against these two failure modes, the insulation of the device must be capable of resisting water and CSF ions indefinitely.

All power consumed by the implanted circuitry must be radiated across the intact scalp through an RF link. To minimize power loss in the scalp tissue and to minimize the hazards of stray leakage currents associated with this, the power consumption of the circuitry should be minimized. To minimize shock hazard, the supply voltage should be kept to a few volts. The minimum power consumption predicted makes it infeasible to use implanted batteries rather than an RF link to power the device.

Any chronic routing of wires through the skin eventually results in infection. Therefore, it is desired to couple

all power into the device and all information out of the device across the intact skin. This requires the use of either inductively coupled RF links or ultrasonically coupled piezo-electric crystal links. The system size requirements regarding these links require that there be only one output data channel. One input power link will be sufficient.

The electrode array and all circuitry except the transmitter and power circuitry will be on a silicon substrate. This chip must be laid across the surface of the cortex between the cortex and the skull. To prevent excessive inward pressure on the cortex, the chip must be no thicker than two to three millimeters. For the same reasons, since the chip is flat and rigid, its lateral dimensions must be no larger than a square centimeter. Because the integrated processing circuitry will likely consume at least half of this area, only one half square centimeter or less remains for the electrode array. This compares to the area of the primary visual cortex accessible for experimentation of crudely between five and ten square centimeters.

The transmitter and power supply circuitry and their associated antenna coils will be located between the skull and the scalp at the back of the head. Wires will feed from these circuits to the electrode part of the implant. Implants as large as 180 by 125 millimeters and 6.5 millimeters thick have been successfully surgically implanted in this same anatomical region (Ref 11). The size of the

transmitter and power supply circuits proposed in this study will be well within these limits.

Because the circuitry and electrodes are all integrated onto a single substrate, a single failure anywhere in the circuitry will require surgical removal of the entire integrated circuit and its replacement or the end of the experiment. Thus, it is a necessity for the implanted circuitry to be simple and reliable and for the insulating package to protect the device from the CSF for indefinite periods of time.

In summary, Kabrisky has proposed a theory on the role of cortico-cortical interconnections in the pattern recognition process of the brain. The problem of this thesis is to investigate the design of a system capable of testing Kabrisky's theory. The requirements of that system have been discussed. In the following section, a design of this system is proposed and its capabilities and limitations estimated.

III. System Design

Introduction

The two major subsystems of the system design, the implanted subsystem and the external subsystem will be dealt with separately in this section. The internal system, the implant, will first be discussed. Its general functioning will be described and the major design decisions involved in the implant will be discussed. Then the requirements of each block will be stated and an equivalent circuit design of that block described. Finally, the control mechanisms of the equivalent circuit design of the entire internal system will be discussed. The external subsystem will then be dealt with in the same fashion, and the capabilities of the internal and external subsystems combined will be described. The matrix electrode of the system described in this section is a twenty by twenty 400 electrode array. This is an arbitrary value chosen to facilitate the discussion which follows.

Internal System

Block Diagram Design. A design that meets the requirements set forth in the previous section for the implanted system is illustrated in block diagram form in Figure 3-1. A multiplexed electrode array of 20 rows and 20 columns records from 400 points over a one square millimeter area of the the visual cortex surface. Each column acts as a 20 to 1

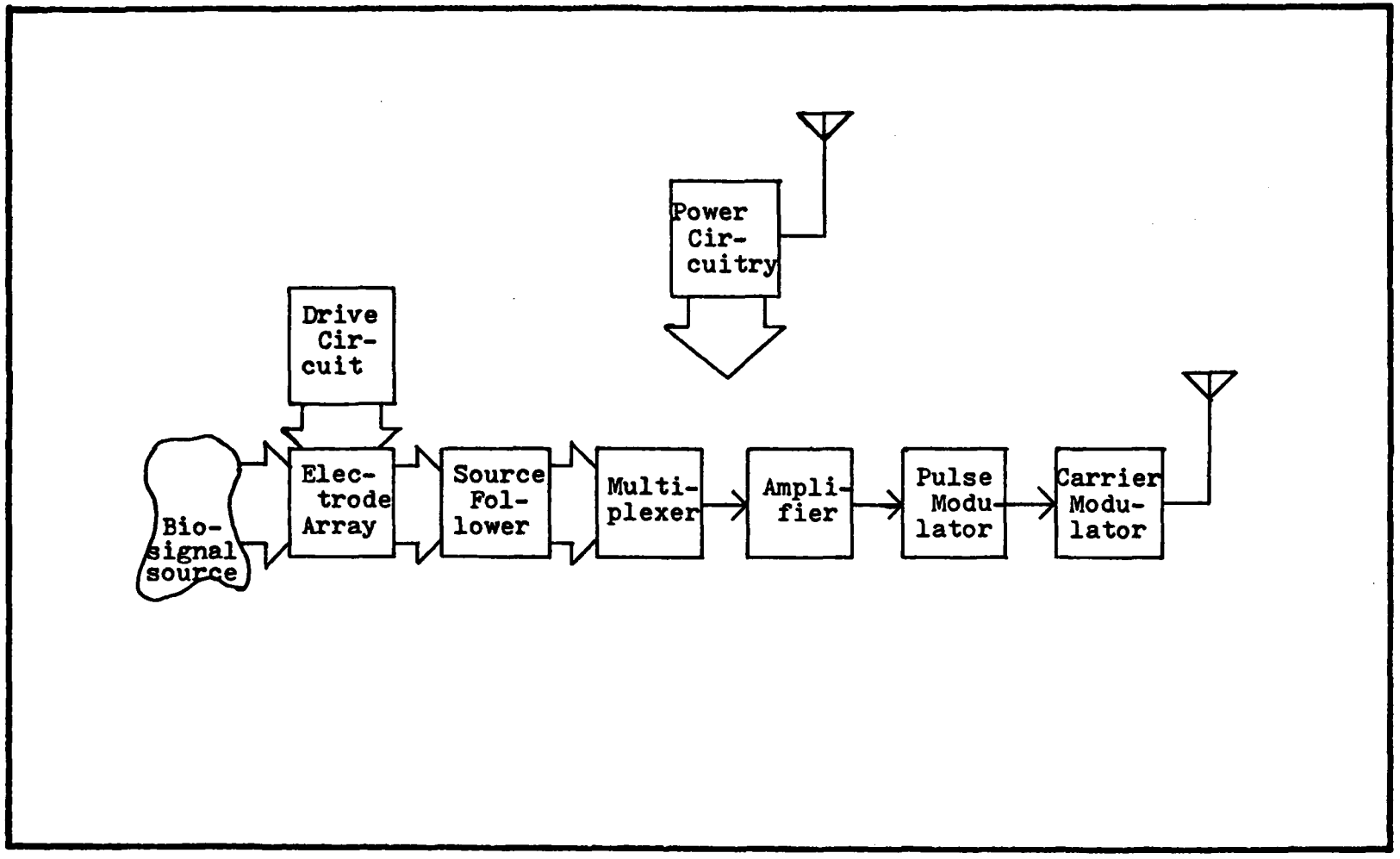

Fig. 3-1. Block diagram of the internal system.

multiplexer with 20 rows of each column being multiplexed onto a single column output line. Under control of the drive circuit, the entire array is scanned 100 times per second. Twenty outputs corresponding to the 20 columns of the array are current amplified by the source-follower amplifiers and are again time multiplexed. All data from the 20 by 20 array is now on a single data line. The 400 data pulses from one scan of the array are amplified and then converted from a pulse amplitude code to a pulsewidth code. The width modulated pulse of each data point from one electrode of the array then turns the oscillator of the carrier modulator on and off to emit a burst of RF the width of which is the width of the data pulse. The RF burst is transmitted and then received by the external system.

A pulsewidth-modulation (PWM) scheme was chosen over placing an entire A/D converter in the implant because the PWM circuitry is much simpler with significantly fewer components and thus requires significantly less substrate area in an integrated circuit. Since the modulator must be integrated onto the substrate of the electrode array, the size of which is critical, PWM was chosen for use in this system. However, because of the advantages of digital pulse code modulation, its incorporation into future systems should be explored. PWM was chosen over pulse-position-modulation because using PWM simplifies the synchronization problem between the internal and external systems, as all

the information for each data point is completely contained in the width of the PWM pulse without reference to any absolute value.

The source-follower amplifiers are simple, single transistor, unity gain amplifiers whose purpose is to reduce noise on the output lines by reducing the output line impedance (Ref 7). Because the output lines affected by these amps are so short in this case, it is not clear that the amplifiers are necessary. Their value in this system should be examined in future research.

For the transcutaneous transfer of data from the implanted to the external system, an RF link was chosen over a piezoelectric crystal ultrasonic link. Pizoelectric crystals, with a maximum bandwidth of a few megahertz, cannot support the necessary bandwidth of this system which will be greater than 15 megahertz. An RF link was also chosen for transmitting power through the skin because of its low transmission loss and high coupling resulting in a transmission efficiency of over fifty percent (Ref 8:473).

Complementary MOS logic was chosen for the integrated circuitry because of its low power consumption.

The decision to matrix multiplex the electrode is discussed in detail in the electrode design section of this paper. The column output lines of the matrix are multiplexed a second time onto a single data line to reduce the number of data channels across the scalp to one. This simplifies the data transmission problem.

Block Design. This part of the section describes in detail the requirements and function of each block of the above system block diagram. The electrode drive circuit will be discussed first, followed by the electrode, the source-followers, the multiplexer, amplifier, pulse modulator, and finally the carrier modulator. Also, a possible equivalent circuit implementation of each block is described.

The electrode drive circuit must perform the scanning of the electrode array. Its function is that of a 20-bit, parallel output shift register with each of its outputs connected to all of the junction field-effect transistor (JFET)gates of one row of the electrode array. Nineteen of the twenty bits of the shift register will always be "1"'s, holding the JFET switches of those 19 rows to the "off" mode. The column output leads therefore, will be reserved for the data from the electrodes in the 20th row which receives a "0" from the 20th bit of the drive circuit shift register and are so in the "on" mode. By shifting the 19 "1"'s continuously through the 20-bit shift register, the rows of the electrode array are turned on one at a time sequentially. Each shift register output must be capable of driving all the JFET multiplexing gates in the row of the array it controls to the devices' pinchoff voltage.

Because the scan time of the array, T_s, is one over 100 Hz, i.e. a dwell time of 10 milliseconds, the output time dedicated to each row of the array, T_r, is 0.5 milliseconds. This requires the shift register to run at a

frequency of 2000 Hz with a shift time very small compared to 0.5 milliseconds.

The matrix multiplexed electrode array must record the biological signal present at each individual electrode and then multiplex the 20 row outputs of each column onto the single column output line. The electrodes of the array must present a low enough impedance to the biological source to record the biopotential. The signal path through the JFET multiplexing switch and up the column lead must have a high enough shunt impedance to ground and a high shunt impedance to noise sources to deliver a meaningful signal to the source-follower amplifiers. The "on" time for each fow of the array, T_r, will again be 0.5 milliseconds. Therefore, the switching times of the JFET's must be much less than 0.5 milliseconds. A complete discussion of the electrode design is found in Section IV.

The primary responsibility of the source-follower amplifiers is to lower the impedance on the output lines between the electrodes and the second stage amplifier in order to minimize crosstalk between the lines and to minimize the effect of neural noise (Ref 7:212-215). If e_1 is the noise on an output line due to a noise source e_n across an insulating boundary, then

$$\frac{e_1}{e_n} = \frac{\omega R_o C}{1+\omega R_o C} \qquad \text{(Ref 7:215)} \quad (1)$$

where C is the capacitive coupling of the noise source to

the line, ω is the frequency of the noise source, and R_o is the output resistance of the source-follower. If e_n is equal to 100 millivolts at 30 Hertz, then it can be calculated that to reduce noise on the line, e_1, to 1.0 microvolts requires R_o to be on the order of 4 kilohms. This calculation is based on the electrode structure discussed in Sections IV and V of this thesis. For reference, 1 bit in the six-bit output word of this system is approximately 8 microvolts.

The source-followers must also present a very high input impedance to the electrode recording structure. A low input capacitance is needed because it acts with electrode capacitance, C_e, of the electrode as a voltage divider. The input resistance, R_{in}, must be minimized because it acts with C_e as a high-pass filter. The biological signals to be recorded are on the order of 20 to 40 Hertz. Given the electrode fabricated in this thesis as an example, R_{in}must be on the order of 100 megohms, as the impedance of C_e at 10 Hertz is 5 megohms. Finally, the source-followers must not contribute significant noise to the very low frequency, bioelectrical signals.

A single transistor amplifier was chosen over a more complicated and higher performance amplifier due to its simplicity and minimal substrate area consumption while still meeting the design requirements. The small substrate area required for the source-followers is important in that there will be one source-follower for each column output line. These output lines will be less than 250 microns apart.

The multiplexing circuitry must time multiplex the 20 column output lines of the electrode onto a single output line that leads to the pulse modulator. The data from a single row of the electrode array will be present at the multiplexer inputs for a little less than T_r, the "on" time of each row during an array scan, because of the switching time between rows. During T_r, the multiplexer must sample each column line for time T_d, the frame width of one data word, that is, T_r divided by the number of electrodes in each row, to form an output frame of length T_r consisting of 20 pulses each of length T_d. Since T_r is 0.5 milliseconds, T_d will be about 0.025 milliseconds. The switching time of the multiplexer switches, then, must be much less than 0.025 milliseconds. One equivalent circuit that fulfills these requirements is shown in Figure 3-2. The shift register controls the FET gates to perform the multiplexing operation.

The amplifier must amplify the amplitude coded pulses from the multiplexer to a level suitable for accurate comparison in the pulse modulator comparator to yield an accurate conversion to pulsewidth-modulation. Potential amplifier designs found in the literature include a nanopower CMOS/bipolar combination device which works on a 2 volt supply (Ref 12) and a micropower (1 volt supply) bipolar device (Ref 13).

The pulse modulator must receive the amplitude modulated signal of the amplifier and convert it to a width modulated pulse capable of driving the carrier modulator. The pulse modulator will have a data word from a single electrode

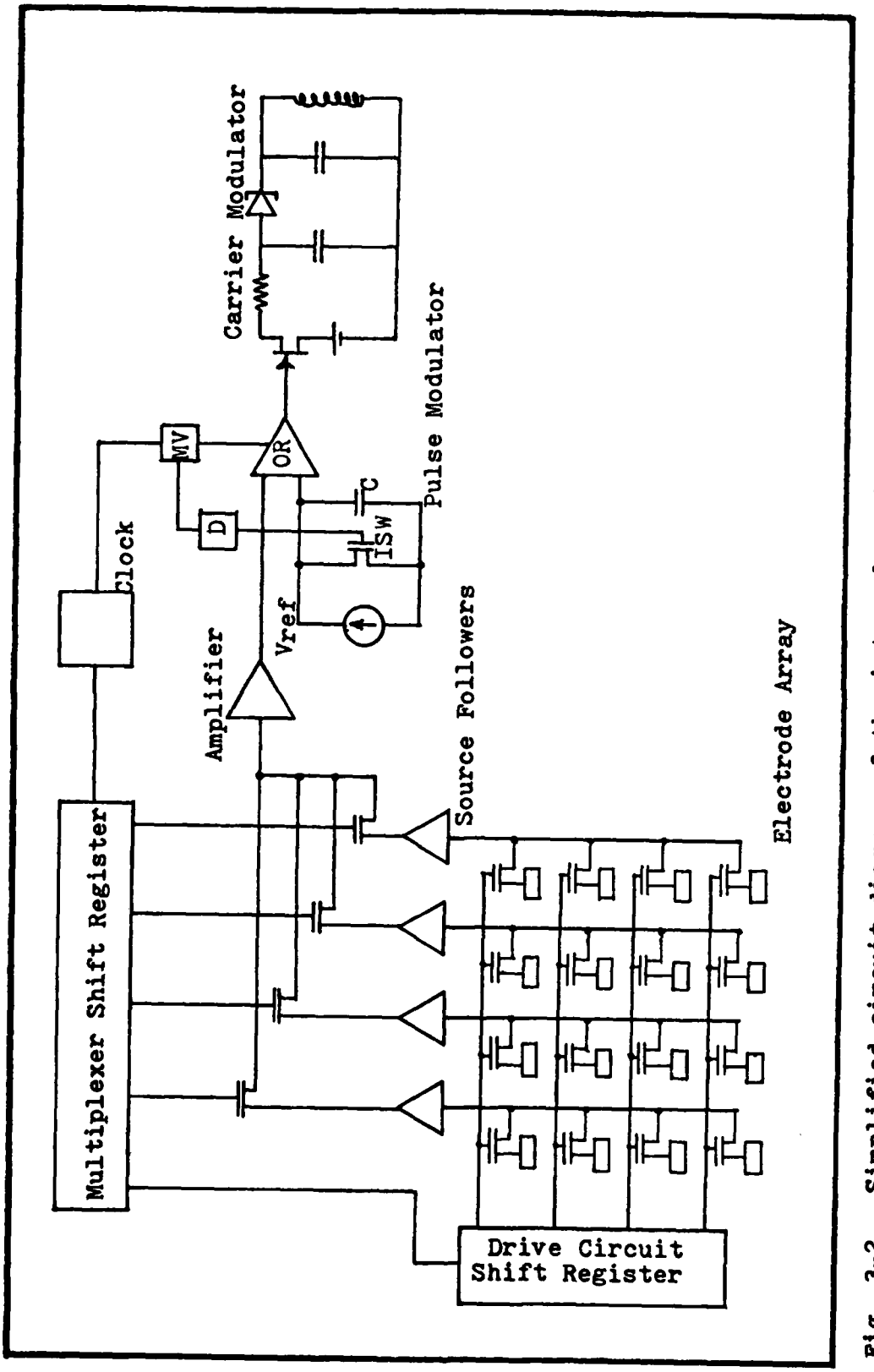

Fig. 3-2. Simplified circuit diagram of the internal system.

of the array available at its input for time T_d (25 microseconds) less the transition time between data words. In this time, the modulator must convert the amplitude pulse to a width-coded pulse of width between some minimum (set to about 20 cycles of the carrier modulator oscillator) and some maximum which is less than T_d.

One possible circuit capable of performing this modulation is shown in Figure 3-2. The same clock pulse that shifts the multiplexer, to place a new data word on the converter input, triggers the multivibrator of the pulse modulator. This releases the override on the comparator sending it to its high output. This is the leading edge of the width-coded pulse. Through a delay, the multivibrator also closes ISW, allowing capacitor C to charge linearly. When the voltage across the capacitor surpasses the amplitude of the analog input, the comparator is driven low forming the trailing edge of the pulsewidth signal. The multivibrator goes low after a time greater than the maximum pulsewidth, thus overriding the comparator and discharging capacitor C (Ref 14:246-249).

The carrier modulator must output a burst of RF oscillation through its antenna of the same width as the width-coded pulses it receives from the pulse modulator. Excellent results have been obtained with implanted transmitters that operate on as little as 240 microwatts (Ref 15). This is suitable for the low power requirements of this system. To encode six bits of data in 25 microseconds, minus the minimum

pulse width and with appropriate spacing between pulses, requires a carrier modulator oscillator with a frequency of greater than 4 megahertz. A transmitter has been developed by Ko (Ref 15) that fulfills these requirements. Though originally designed for FM, the oscillator is convertible to a PWM scheme (Ref 16).

The internal power supply must receive RF radiated power from the external power supply across the intact skin through an RF link. The total power consumption of the implanted circuitry should be less than 10.0 milliwatts at 3 volts DC for an implant containing as many as 10,000 electrodes. The derivation of this value is in Appendix B. These requirements could be significantly reduced by recent advances in nanopower and micropower operational amplifiers and linear/digital integrated circuit combinations operating with supply voltages as low as 1 volt (Ref 12;13). To be biocompatible, the power supply must be failsafe against stray voltages and not heat the tissue between the internal and external coils through transmission losses. A design procedure for such power supplies, including a design example which fits the needs of this system, has been published by Ko, et al (Ref 17).

An alternative possibility for the implanted power supply is the use of nuclear, radioisotope batteries. Nuclear batteries have been experimented with which produce around 500 microwatts of power at about 0.5 volt. These batteries have a life expectancy of nearly 10 years when used in cardiac

pacemakers (Ref 18). As the development of micropower, low voltage integrated circuits continues and as the power and voltage levels of radioisotope batteries improve, it may become feasible to replace the RF power link of this system design with an implanted nuclear battery.

Circuit Design. The block by block pieces of circuitry described in the previous portion of this section function together as a system that fulfills the system design requirements as shown in Figure 3-2. There are two basic control mechanisms that coordinate the individual blocks into a functioning system. One involves the coordinating control of the electrode drive circuit with the multiplexer, and the other involves the interaction of the multiplexer and the pulse modulator. The timing of the latter control mechanism is illustrated in the timing chart in Figure 3-3. Briefly, the multiplexer shift register actually has 21 bits. The 21st bit of the multiplexer shift register acts as the clock for the drive circuit shift register. As the multiplexer shift register shifts the "on" bit through the first 20 positions of the register it samples the data on the 20 column output leads from arbitrary row K of the electrode array. When the multiplexer shift register shifts the "on" bit into the 21st position, it does not sample data, but triggers the drive circuit to shift to row K+1 and the sampling procedure repeats. This control mechanism ensures the coordination of the two shift registers as well as providing a delay time for the column outputs from row K+1 to settle after shifting.

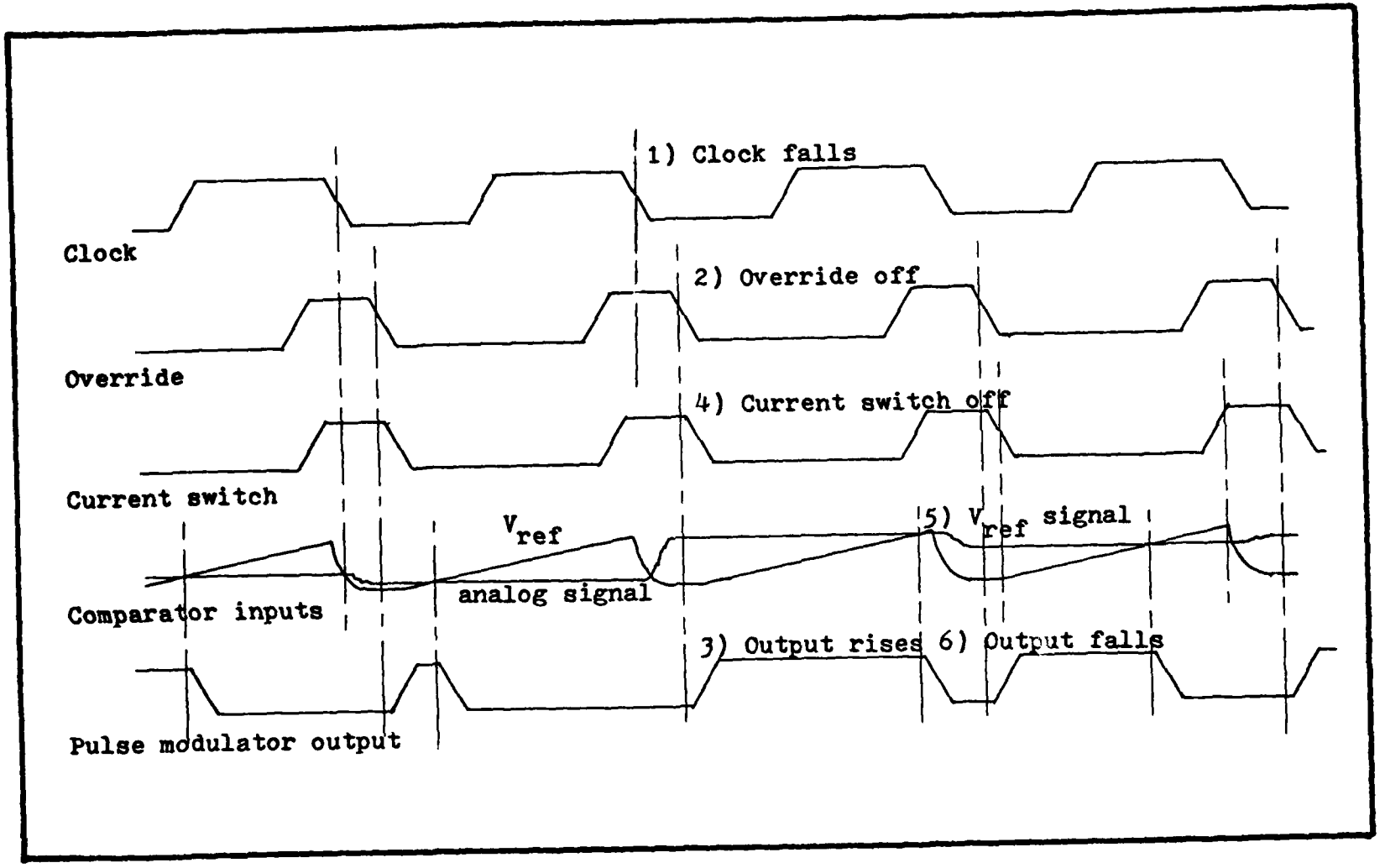

Fig. 3-3. Timing diagram for the pulse modulator circuit of the internal system.

The control mechanism between the multiplexer and the pulse modulator has been discussed previously in the description of the pulse modulator block.

The size of the integrated circuit portion of the implant can be kept well within the limit set by the system requirements of one square centimeter. With an electrode array as large as 10,000 electrodes the integrated circuit containing the array and the modulating circuitry will contain less than 5000 equivalent gates. Assuming a CMOS density of 70 gates per square millimeter, the chip will have to support approximately only 0.7 square centimeters of circuitry.

The implanted power supply circuitry and the transmitter (carrier modulator), which will be located extracranially between the skull and the scalp, have a maximum combined lateral dimension of 28 millimeters in either direction and a total thickness of less than 2 millimeters based on examples from the literature (Ref 15; 17). This is well within the limits of the system requirements.

External System

Block Diagram Design. A block diagram of a system that meets the requirements for the external system is shown in Figure 3-4. The RF burst produced by the implanted system's transmitter is received by a pancake coil lying on the scalp. The received signal is passed through a band-pass filter to remove noise frequencies, amplified, then converted back to a width-coded pulse by the demodulator. The slicer

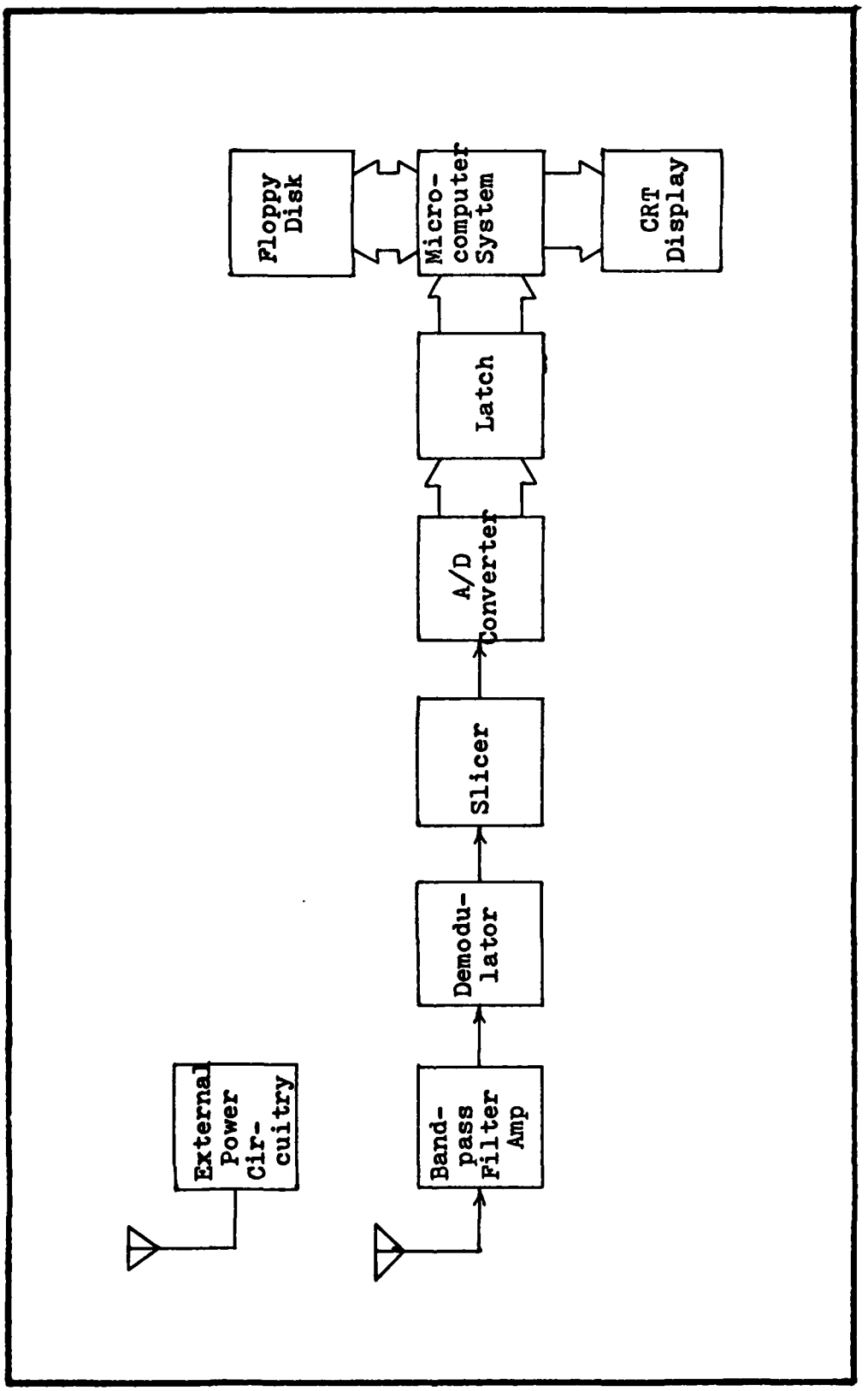

Fig. 3-4. Block diagram of the external system.

straightens the edges of the pulse and amplifies it to a level suitable to drive the digital circuitry of the pulsewidth A/D converter. The digitized data word is then latched into the microcomputer which stores the data in RAM in real time. After an experimental event (data recording session), the microcomputer dumps the RAM data onto a floppy disk. The microcomputer also controls the display of some portion of the data in real time onto the CRT display. The remainder of this part of the section deals first with a discussion of the major decisionsmade in the design of the external system, followed by a description of the requirements and implementation of the blocks of the system. Finally, the coordination of the external system will be described.

A pulsewidth modulation A/D converter normally takes an amplitude modulated pulse, converts this to a width modulated pulse, then converts this to a digital output (Ref 16). This system design divides this task into two portions. The first conversion takes place in the implanted circuitry as the analog signal level recorded by the electrode array is converted to a width-coded pulse then transmitted out of the body. The pulsewidth to digital conversion takes place in the external system. Therefore the pulsewidth A/D conversion scheme works very well with this system.

It would be most convenient to have the microcomputer store the data received from the internal implant onto the floppy disk in real time and also to have the microcomputer

control the external system. The rate of data storage onto the floppy disk, however, is prohibitively slow. Therefore, the system was designed to have the microcomputer store the data on RAM through a direct memory access (DMA) channel in real time, then after a short data collection session, to dump the RAM data onto the floppy disk.

Block Design. The following pages discuss the functional requirements of the blocks of the block diagram of the external system and suggests some possible equivalent circuit implementations of these blocks.

The band-pass filter, demodulator, and slicer circuitry must receive the RF burst transmitted from the implanted system, filter out noise frequencies, pick off the envelope of the RF signal, and shape the pulse into one suitable for driving the digital circuitry of the A/D converter. Through all this the width of the pulse must be accurately maintained. A data rate of $1/T_d$ (frame length of one data word) must be handled and the response time of this circuitry must be much less than T_d.

An equivalent circuit diagram of a design that meets these requirements is shown in Figure 3-5. Tank circuit RLC acts as a band-pass filter receiver to remove noise from the signal. R_d and C_d act together with the detector diode as a low-pass filter to pick off the envelope of the RF burst while C_{d2} blocks any DC offset in the signal. The Schmidt trigger shapes the pulse to suitably drive the NAND gate of the comparator of the A/D converter.

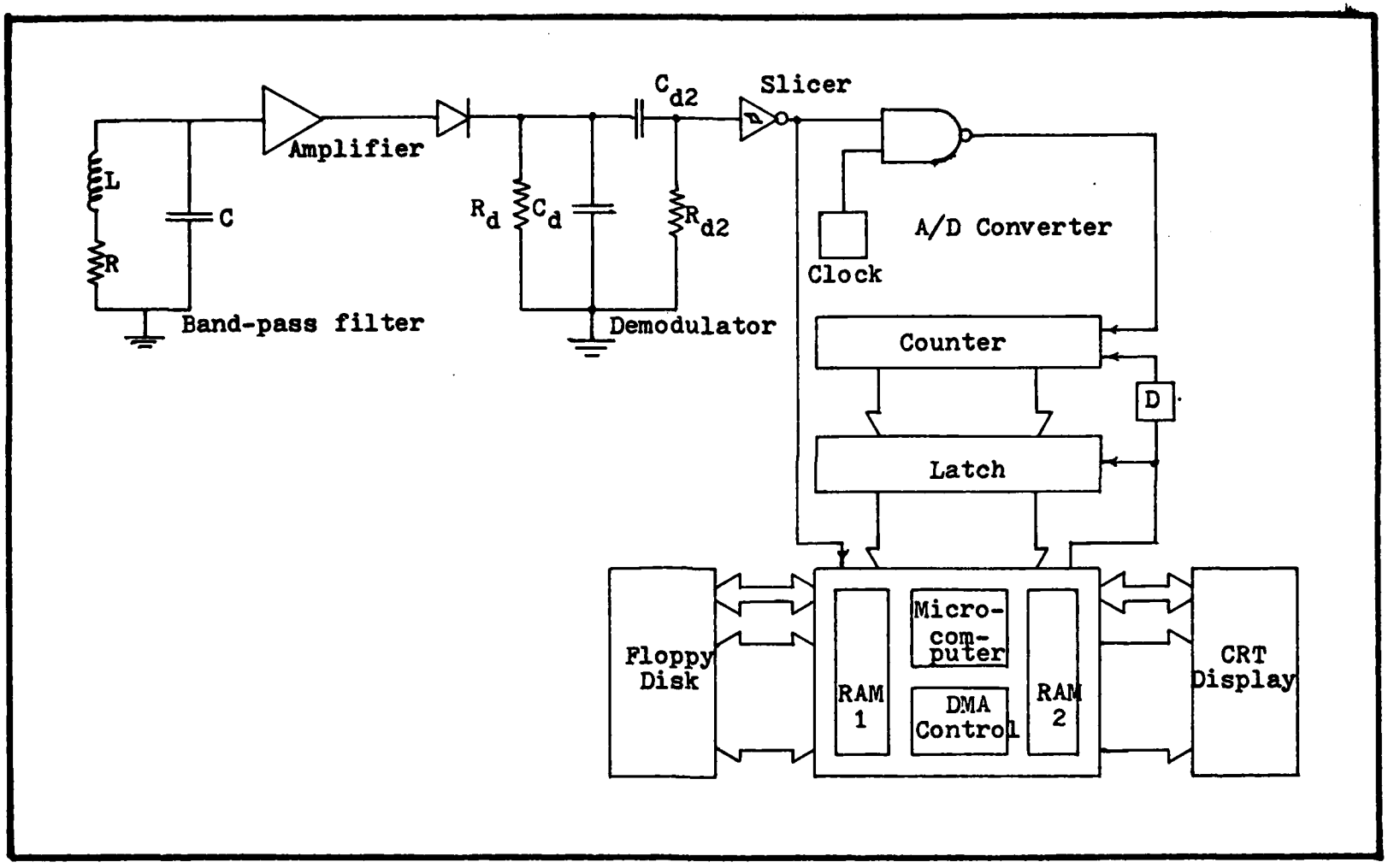

Fig. 3-5. Simplified circuit diagram of the external system.

The pulsewidth A/D converter and latch accept the width modulated digital pulse from the slicer, digitize it, and enter the digital data word into the latch to be read by the microcomputer. The A/D conversion is to six-bit accuracy. The converter must be able to handle $1/T_d$ conversions per second.

An equivalent circuit that meets the converter and latch requirements is shown in Figure 3-5. The width modulated pulse from the slicer is NANDed together with a clock. This forms a train of pulses the length of which is the length of the input pulse. These pulses are counted by the counter and the resulting digital data word is entered into the latch (Ref 14). This design requires a counter that can count at a frequency of one over the maximum variation in pulse width times two to the number of bits accuracy needed. Since the maximum pulse width is approximately 20 microseconds and six-bit accuracy is desired, a counter frequency of approximately 3.2 megahertz is needed.

The microcomputer system, including the microcomputer, RAM memory, direct memory access (DMA) channels and control logic, a floppy disk, and a CRT display, must read the data words from the A/D converter latch and store these onto RAM in real time through a DMA channel. A simple control system that coordinates the external system is shown in Figure 3-5 and its timing chart in Figure 3-6. The microcomputer tests the slicer output to detect the trailing edge of the width-coded data pulse. When the trailing edge

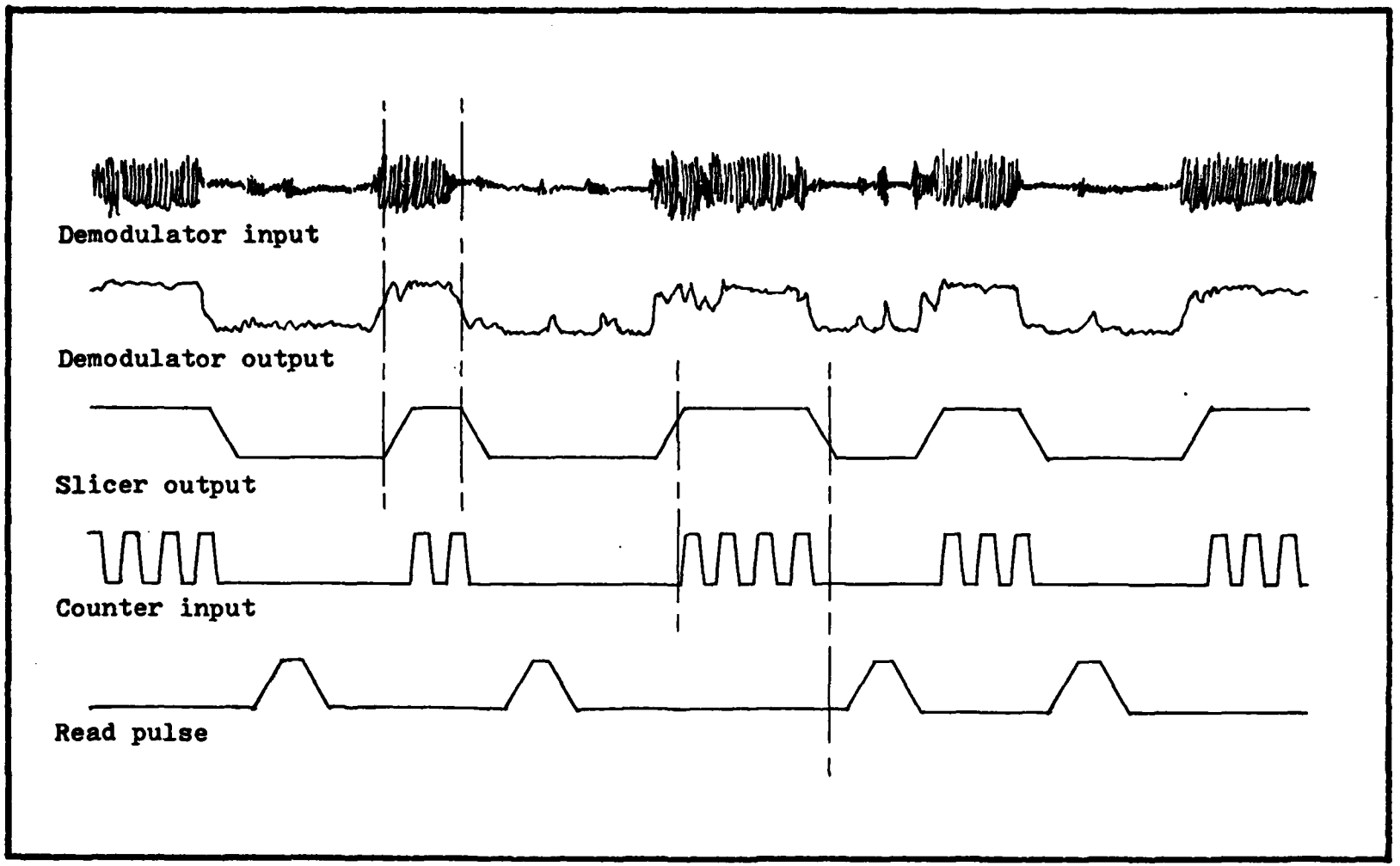

Fig. 3-6. Timing diagram for the external system.

is detected, the microcomputer strobes the latch, reads the data, and acting through a delay resets the A/D converter counter. The A/D converter is now ready to receive another data point.

At the end of a specific test event, the RAM data is dumped onto the floppy disk by use of another DMA channel under control of the microcomputer. The extremely high data rate desired, 1 megahertz word rate, will require the use of the high speed data routing capabilities of bit-slice microprocessors for the DMA channels and control logic.

With one bank of RAM, no data gathering can take place while the RAM is being dumped onto the disk. However, the system could be extended and its flexibility improved by adding another RAM bank as shown in Figure 3-7 so that one RAM bank will be available for testing while the other is being dumped onto the disk.

Storing the test data in this fashion severely limits the recording length of a test event due to limits on the size and availability of RAM. Considering the use of the device, the desirable test length is in a range of 1 to 3 seconds based on the length of the response of the cortex to visual stimuli reported by DeMott (Ref 9). Therefore, for a 100 by 100 electrode array system and a 100 megahertz word rate (six-bit words), between six and eighteen megabits of RAM would be required. The technological and financial expense of this amount of RAM could prove prohibitive.

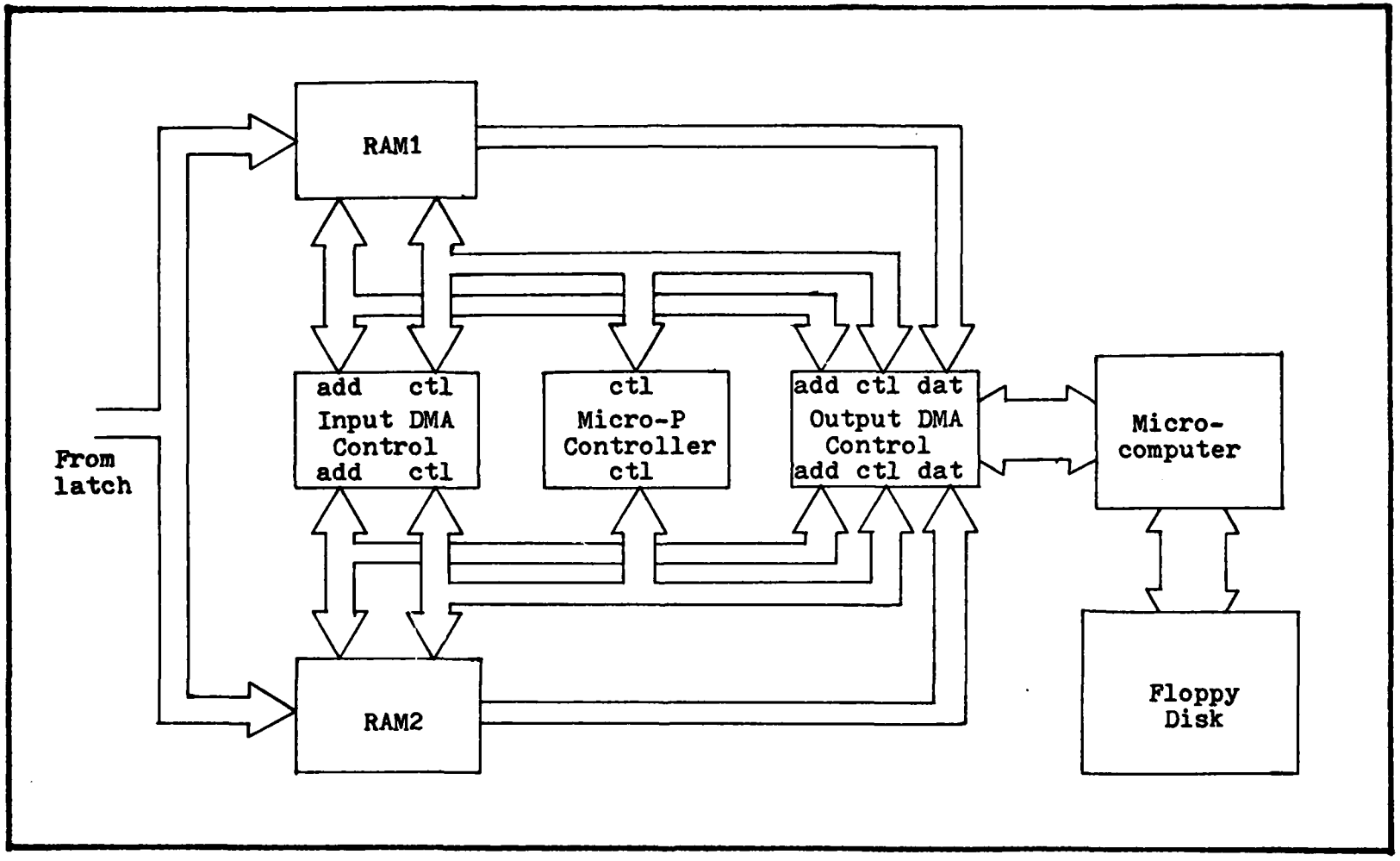

Fig. 3-7. Proposed data storage scheme for the external system (Ref 19)

A realistic approach to the problem would be to begin with a relatively small electrode array system, possibly 20 rows by 20 columns, and a reasonable amount of RAM for data storage. This system could then be extended depending on the usefulness and significance of the data being collected.

System Data Rate. In estimating the system data rate it is first assumed that the data rate will be limited by the internal system. This is due to the strict requirements on power and voltage levels, biocompatibility, and size for the internal system which do not apply to the external system. Also, it is assumed that the internal system's maximum data rate will be set by one of the more complex components of that system, the shift registers or the operational amplifiers.

To achieve a data rate of one million six-bit words per second (data frame of length 1.0 microsecond) to be modulated onto a carrier frequency of 100 megahertz with a minimum pulse width of 10 oscillator cycles, the pulsewidth-coded output word will be in a range between 0.10 and 0.73 microseconds. This leaves 0.27 microseconds of the data word frame for transition between data values.

Assuming a data level range of 0.0 to 1.0 volt in the amplifier and pulsewidth modulators, the operational amplifiers must, therefore, be capable of a slew rate of 1.0 volt per 0.27 microsecond or 3.7 volts per microsecond.

Micropower amplifiers have been built which surpass this slew rate (Ref 12). CMOS shift registers are commercially available (Ref 21) which achieve clock rates greater than 1 megahertz with propagation delays less than 270 nanoseconds. Thus a 1 megahertz data rate is feasible for this system.

In summary, a system which meets the requirements set forth in Section II has been proposed. Its feasibility and its capabilities and limitations have been discussed. Sections IV and V will deal with the design and fabrication of a prototype multiplexed electrode array, the central component of the system of this section. The results and conclusions drawn from the system design will be discussed in Sections VI and VII.

IV. Electrode Design

Introduction

The concluding discussion on the first problem of this thesis, the system design, will be found in the last two sections of this paper. The remainder of the paper, but for these ending sections, will deal with the second problem of this thesis, the design, fabrication, and evaluation of the multiplexed array microprobe. The problem is to design a multielectrode array capable of simultaneously recording the electrical signals existing over a specific surface area of the visual cortex. The multielectrode probe design arrived at should be extendable to thousands of electrodes and to a sufficiently large area of the cortex to adequately investigate Kabrisky's theory (Ref 2). This probe will fulfill the requirements of the electrode block of the system design of Section III. Only those aspects of the electrode design that affect the ability of the electrode to fulfill those requirements will be discussed in detail.

In this section, the problem will first be analyzed, then the specific objectives of the design will be stated. An explanation of design decisions arrived at will then be followed by the development of the junction field effect transistor (JFET) design, the only component of the probe design which needs to be discussed separately. In finishing, the final structure arrived at through the design process will be shown with a description of its electrical characterization.

Problem Analysis

As reported in detail in the Problem Analysis and Theory section of this thesis, the system problem is to record the electrical signals existing over a large surface area of the visual cortex areas to investigate the possibility that the average membrane potentials over these surfaces, a summation of the EPSP's and IPSP's, perform the reinforcement and interference necessary if the cortico-cortical interconnections are indeed performing a Fourier transform computation as a sub-task of their pattern recognition processes (Ref 2). Due to the highly localized interconnections between neurons in the horizontal plane of the areas of the cortex, the resolution of the multielectrode array of a device to test this theory should be on the order of 0.05 to 0.5 millimeters to yield sufficient data.

The summation of the membrane potentials of the neurons of the cortex emits a bioelectric field into the cerebrospinal fluid (CSF) that has an average peak to peak amplitude of 200 to 400 microvolts over a bandwidth ranging from less than 1 to a maximum of 40 or 50 Hertz. The metal-electrolyte interface, formed by the metal electrode placed in the electrolytic CSF, that must record this field is highly capacitive. The electrons of the metal and the ions of the CSF form an electrical double layer called the Helmholtz layer. This double layer acts as a capacitor with a dielectric constant of approximately ten and a thickness on the order of an atomic radius of only two to four angstroms. The

calculated capacitance of this interface is approximately 2 picofarads per square micron. The exchange current of this interface ranges from 10^{-9} A/cm^2 for gold electrodes and 10^{-8} A/cm^2 for platinum electrodes to 10^{-5} A/cm^2 for silver electrodes (Ref 7:214). This minute current component results in the interface being almost entirely capacitive. It has been observed that tissue response to a metal electrode increases with increasing exchange current. Therefore gold and platinum are among the best metals for chronic implantable electrodes and silver among the worse (Ref 22: 242-243). For stimulating electrodes, platinum has proven to be superior to gold (Ref 5:496).

In summary, the problem is to record, through capacitive coupling, bioelectrical signals with an amplitude of 200 to 400 microvolts and frequency content of 1 to 40 Hertz over the surface of the visual cortical areas. These signals must be recorded simultaneously by an electrode array with an interelectrode spacing of 0.05 to 0.5 millimeters.

Requirements

Objectives. The objectives of the design of a device that satisfies this problem are as follows.

1) A multiplexed matrix electrode array, extendable to thousands of electrodes, capable of being scanned at a 100 Hertz rate.

2) A high shunt impedance to electrode impedance ratio.

3) Low noise at low frequencies.

4) A structure capable of short-term reliable operation in the saline bath environment of the CSF.

5) A structure that does not alter the functioning of the cortex electrically, chemically, or mechanically.

6) Low voltage operation.

Specific Requirements. In accordance with the system problem, this probe must record simultaneously from an array of electrodes spread over as large an area as possible of the cortex. Since this array will eventually be extended to hundreds or even thousands of electrodes in future development, a design involving one output lead for each electrode soon becomes infeasible. The massive number of output leads required would take up a huge portion of the substrate surface area of the integrated circuit electrode array making achievement of the appropriate electrode resolution difficult if not impossible. This would also introduce huge crosstalk problems between the output leads. These difficulties led to the idea of a multiplexed electrode array with all electrodes of a column of the array multiplexed onto a single column output lead by the use of a multiplex switch associated with each electrode in the array (Ref 23). An integrated driving circuit would turn on the multiplex switches of one row of electrodes, at which time the signals from this row of electrodes would be the only signals on the column output leads.

In this situation, the multiplex switches must be transistors which in turn requires that the substrate upon which the electrode array is built be silicon. This is

necessary to facilitate the use of standard integrated circuit technology in the fabrication of the device. In order to test the feasibility of the multiplexed array idea, while limiting the fabrication difficulty in this first attempt, a four by four array was decided upon for the electrode array design of this thesis. An interelectrode spacing of 250 microns is used in order to compare our results with those of previous experiments in this area (Ref 9).

In order to record a meaningful signal at the outputs of this device, an attenuation of less than 3 dB is desired. Therefore, the ratio of the device shunt impedance to electrode impedance (the impedance of the electrode-electrolyte interface) must be greater than one. The attenuation is a result of the shunt capacitance acting with the capacitance of the metal-electrolyte interface as a voltage divider. To maximize the shunt impedance, the width of the output leads is kept to a minimum. More importantly, maximizing the individual electrode area increases the electrode capacitance and thus decreases the electrode impedance. The electrode area is limited by the size of the multiplex transistor associated with each cell and the desired interelectrode spacing.

Because the recorded signal is on the order of a few hundred microvolts, device noise should be no more than a few microvolts. The two major sources of noise in the structure will be capacitive coupling between output leads and capacitive coupling between the output leads and membrane potentials

of neurons lying alongside the device. grounding the substrate below the output leads, the effects of the neural noise can be kept well within the required limits. This is because the shunt capacitance to ground is much higher than the shunt capacitance to the neural noise sources. The output leads are far enough from each other in the design of the device that their interlead capacitive coupling is much smaller than the shunt capacitance of theleads to ground.

The requirement of short-term reliable operation in the CSF environment is very important. The saline bath of the CSF degrades the performance of the electrode array, especially of the transistor multiplex switch devices. It does this as the CSF ions diffuse into the device surface causing increased leakage current of p-n junctions and introducing other parasitic surface effects. In order to record meaningful physiological data, the electrode array probe should have nearly identical parameters for at least the duration of a few hours of testing. To achieve this the active areas of the probe will be insulated with a chemically deposited silicon dioxide layer. The bonding areas will be coated with a moisture-proof epoxy and the wires with an insulating lacquer.

For several reasons we wish not to damage or alter the functioning of the test animal's cortex during in vivo experimentation with this device. In addition to the obvious humane reasons, the animal must be kept as intact as possible as other experimenters will be working on the same animal. In terms of this thesis, decreasing the interference with the

test subject's tissue increases the meaningfulness and validity of the results. Also, it is desired to begin preparing for the stage of this research program when a data recording and transmitting device will be chronically implanted.

There are three basic mechanisms of damage or alteration of functioning of the tissue: electrical, chemical, and mechanical. Electrically, the supply voltage lines to the transistors must be well insulated from the CSF to reduce shock hazards. Also, the metal chosen for the electrode must have a very low exchange current to minimize tissue damage as explained in the problem analysis portion of this section. To prevent any chemical damage to the biological system, insulating materials which package the device must be chemically inert in the saline bath of the CSF. To guard against any mechanical damage or alteration of the functioning of the cortex, the array substrate must be kept physically small in the horizontal plane, to about one square centimeter, to prevent the flat substrate surface from flattening the curved surface of the cortex.

The probe must be a low power, low voltage device to minimize shock hazards to the animal and for ease of encapsulation. Also, eventually, all power will be radiated in through the intact scalp. Low power is therefore desirable to minimize this design problem. Three volts is arbitrarily chosen as a limit on the supply voltage in this design, which is typical in present-day implanted systems.

This will probably be reduced in future devices since integrated circuits have been recently developed which operate on less than one volt (Ref 19).

Explanation of Design Decisions

The next several paragraphs describe the reasoning leading to the various design decisions arrived at in the developing of the microprobe structure. These decisions deal with overall circuit considerations, choice of device for the multiplex switch, and choice of materials for the structure fabrication and for the insulation.

The decision to use a multiplexed array with only one output lead per column, rather than a nonmultiplexed array with one output lead per electrode, was made in consideration of future designs which will include hundreds and possibly thousands of electrodes. For an array of a thousand electrodes, at one output lead per electrode, the surface area available for the electrodes themselves and the integrated circuitry would be significantly reduced. Also, with this many leads closely spaced, the crosstalk problem among them would be difficult to resolve. The multiplexing of the device, however, results in the addition of one multiplex switch associated with each electrode. Given the room allowed for each electrode-switch cell by the interelectrode spacing requirements, this switch must be a transistor which in turn requires a silicon substrate. Further, the matrix layout of the array calls for the use of diffused crossovers to reduce the metallization steps to one.

The use of transistors as switches in the multiplex array adds complexity to the design and fabrication of the electrode array and adds noise to the signal as it passes through the transistor. Also, the resulting use of silicon as a substrate requires that the substrate be kept smaller since silicon is not flexible. The array could otherwise be built upon a flexible substrate and so be larger in size as it could fit more easily over the curved surface of the cortex without flattening it.

The decision to limit the size of the array to four by four was made in order to keep the device simple yet still adequately test the feasibility of the multiplexed matrix design. The electrodes themselves were designed to be rectangular and as large as possible to maximize their area and thus the capacitance of the electrode with the CSF. This results in better coupling to the biological signal source and less attenuation of the recorded signal by the device. This increasing of the area of the electrode also increases the number of neurons in the summation of bioelectrical signals recorded by each electrode. The effect of this on the meaningfulness of the data is not known. Approximately 1600 neurons lie in the 2 millimeters of cortical volume below each electrode of the present design.

The considerations of the above paragraphs led to the equivalent circuit of the electrode array shown in Figure 4-1.

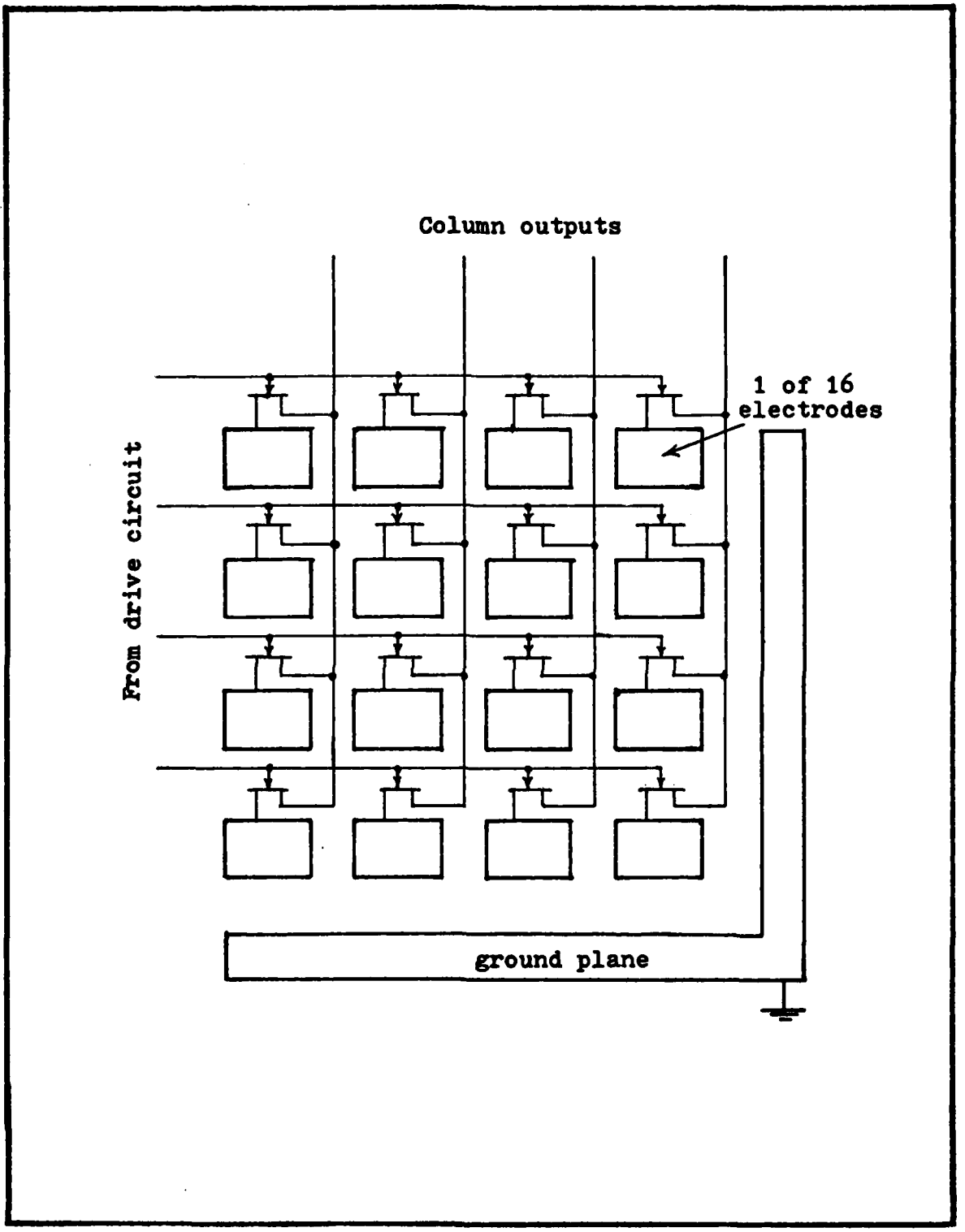

Fig. 4-1. Four by four multiplexed electrode array circuit diagram.

A JFET device for the multiplex switch was chosen over either a bipolar or a MOSFET device. Strictly, the MOSFET might be the better device choice, but it is more difficult to fabricate successfully and its dependence on surface effects make the MOSFET very susceptible to the degrading effects of the ionic CSF. A JFET is chosen over a bipolar device for several reasons. The JFET is superior in the microvolt signal range due to its high DC isolation between input and output and thus negligible offset voltage. Also, the JFET is a majority carrier device and electrically looks like a resistor in the "on" mode. The bipolar transistor is a minority carrier device and the signal must pass through two p-n junctions in the "on" mode. This results in the JFET being far superior in noise immunity in the microvolt signal region (Ref 24:179; 25:156-158). The extremely high input impedance of the JFET yields a much lower power consumption than a bipolar device. The JFET is also easier to fabricate in that it involves only one critical diffusion. The disadvantage of using a JFET is that the bias voltage must be applied to hold the device off which is the default mode in the usage of this project. Figure 4-2 displays one of the sixteen JFET-electrode cells.

Silicon was chosen as the substrate material because silicon transistor technology is well developed. However, a flexible substrate would be better for our purposes, as it could fit better over the curved cortical surfaces without

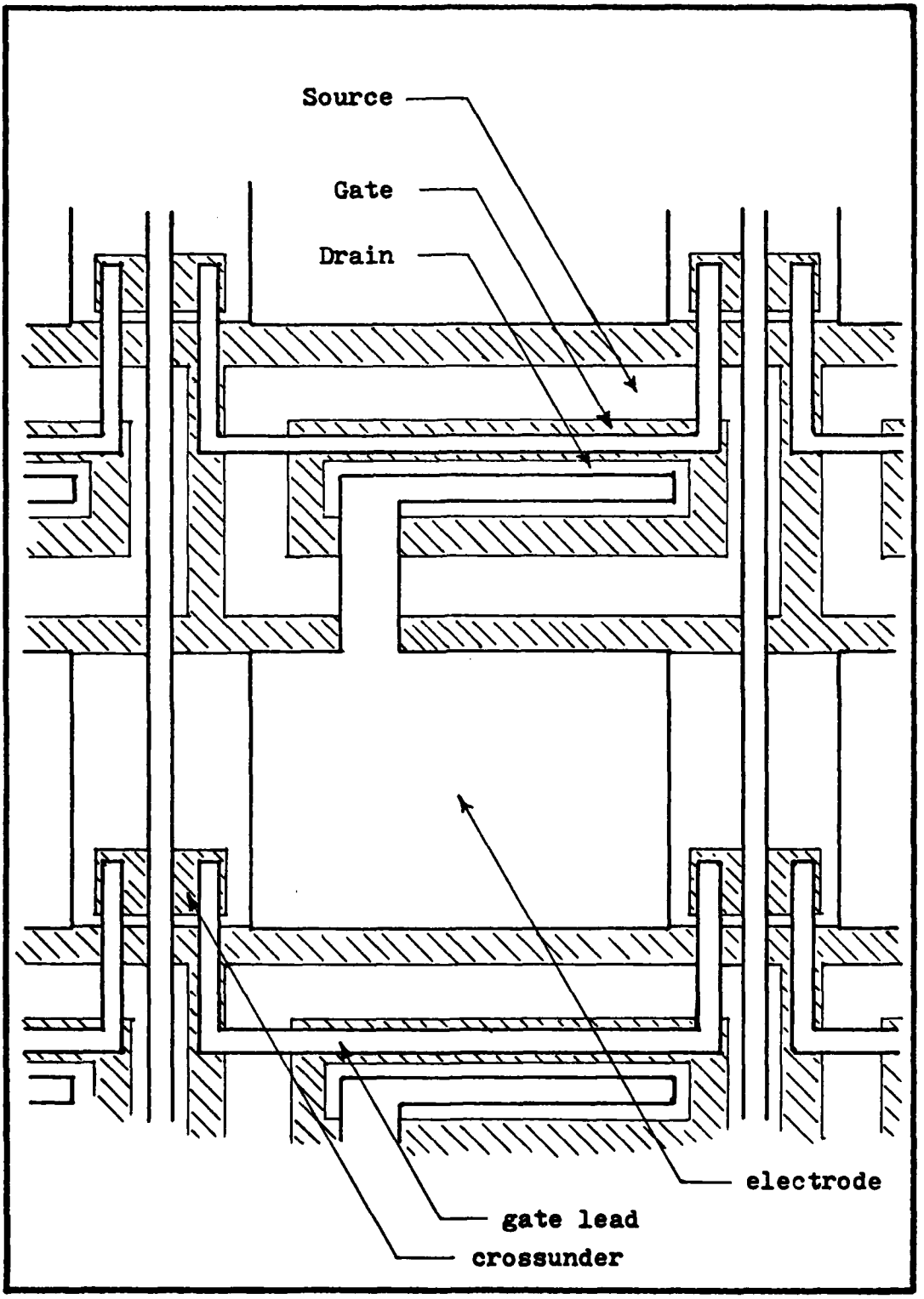

Fig. 4-2. One JFET-electrode cell of the multiplexed electrode array.

flattening the cortex. This would allow the use of a larger array. The choice of gold for metallization was made on the basis of its inert behavior in the CSF environment. Of the three metals that exhibit this inertness in the CSF, gold, platinum, and stainless steel, gold is the easiest to work with using standard integrated circuit techniques. As mentioned earlier, tissue response increases with increasing exchange current of the metal-electrolyte interface. The exchange current for the gold-electrolyte interface is approximately 10^{-9} A/cm^2 which is very low compared to other metals. The exchange current for silver approaches 10^{-5} A/cm^2 (Ref 22:242-243).

The insulation layer over the active surface area of the device must be accurately cut to expose the microelectrode surfaces. This stipulates the use of an insulating material which can be selectively removed using photolithographic methods. Silicon dioxide was chosen for this insulation layer because of its well developed technology and its adequacy in protecting the device from the CSF for short periods of time. The use of silicon nitride for this purpose should be examined in future development as it forms a higher quality insulation layer than silicon dioxide and can also be selectively etched using photolithographic techniques. The silicon dioxide layer can be improved by annealing it, which increases its density and thus improves its insulating abilities (Ref 5:496). This cannot be done, however, with the gold metallization, as the gold evaporates below the

silicon dioxide annealing temperature. The use of platinum for metallization avoids this problem. Here, the silicon dioxide can be annealed without vaporizing the platinum metal layer, but platinum is much more difficult to work with than gold. Therefore, gold was chosen as the metallization in this device.

Once the lead wires are soldered to the bonding pads around the periphery of the device, the bonding pads and solder connections must be insulated. The insulation procedure here is to coat the areas with "moisture-proof" epoxy then cover this with a layer of medical grade Silastic for biocompatibility (Ref 8:477-478). There are several potentially useful similar insulation procedures found in the literature (Ref 10). These should be experimented with in future studies.

JFET Design Development

The JFET multiplexing switch is the only component of the multielectrode microprobe that requires special consideration in its design. The following paragraphs describe the development of that JFET design. First, the objectives of the device are listed, then the development of the important device parameters is described.

Objectives.

1) Minimal on resistance of the device, R_{on}. R_{on} should not significantly increase the resistance of the output line.

2) A device off resistance, R_{off}, that is high enough to effectively open the output line in the "off" mode.

3) Sufficiently fast switching time. This is not too important in this design, but will be very important in future designs when possibly a hundred electrodes are multiplexed onto a single column line.

4) Noise added to the signal passing through the device of no more than a few microvolts. Because the JFET is a majority carrier device, and electrically looks merely like a resistor in the "on" mode, this requirement is automatically met.

5) A pinchoff voltage of less than 3 volts, per the electrode design requirements. The pinchoff current, I_{goff}, should be a minimum to minimize power consumption.

Design Development. Figure 4-3 shows a cross section of a JFET and some of its more important parameters. All parameter values derived in this section are estimates. The exact values will be determined by the starting material available, the mask set, and processing considerations. In this design, the most important of the performance parameters is R_{on} which is to be minimized. It can be shown that (see Appendix C.):

$$R_{on} = \frac{d}{V_p}\left(\frac{1}{2k\mu_{ch}}\right)\frac{L}{Z} \qquad (1)$$

where all symbols are defined in Figure 4-3. For the allowable values of V_p and d in this design, the channel mobility is nearly constant. Also, the channel length and width, Z and L, can be varied independently of V_p and d.

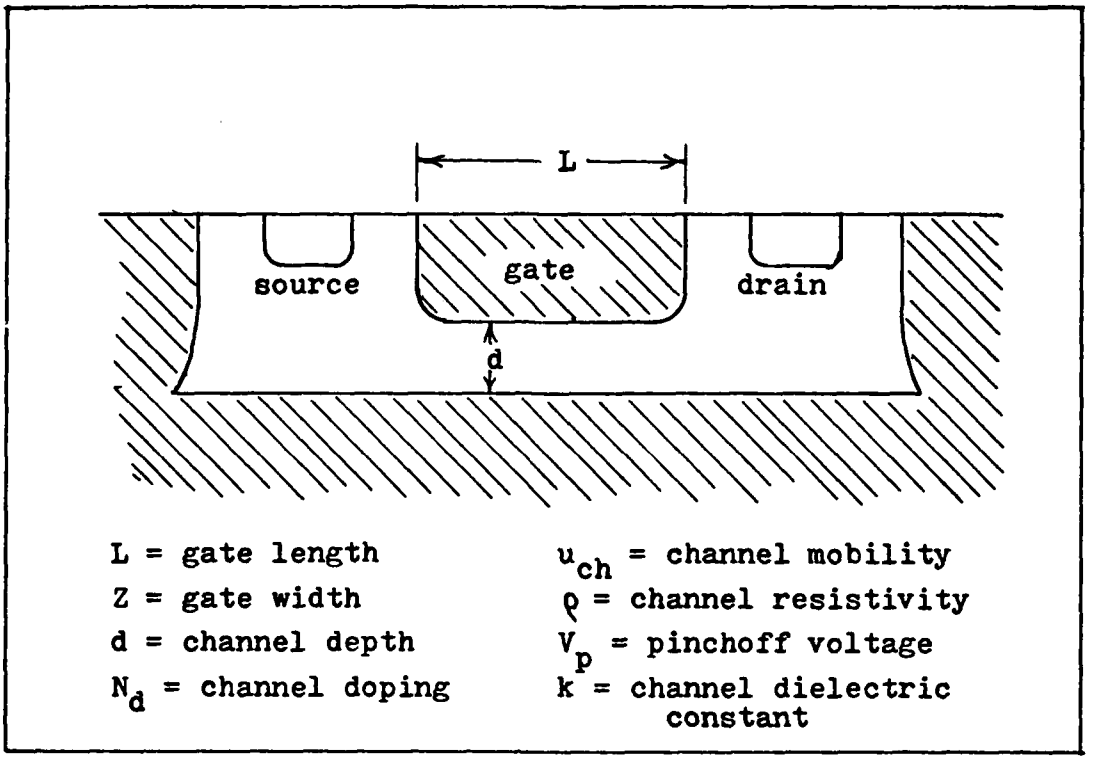

Fig. 4-3. The basic JFET structure.

Therefore, to minimize R_{on}, V_p is made as large as possible and d is made as small as possible. Thus, V_p is chosen to be 3 volts per the design requirements and d is chosen to be 1.0 micron, its smallest possible value without unduly increasing the complexity of fabrication.

With the pinchoff voltage and channel depth set, the impurity concentration of the channel is fixed and can be calculated by a rearrangement of the pinchoff voltage equation:

$$V_p = \frac{d^2 e}{2k}(N_d) \qquad \text{(Ref 26:271)} \qquad (2)$$

to be 4×10^{15} cm^{-3} which results in a channel resistivity of 1.3 ohm-cm.

Now,

$$R_{on} = \frac{\rho L}{Zd} \qquad (3)$$

With the channel depth and resistivity fixed, to further minimize R_{on}, the Z to L ratio should be maximized. The minimum L, due to the 5 micron rules used in designing the device, is 15 microns. The interelectrode spacing desired and geometrical considerations limit Z to 580 microns. This yields a Z to L ratio of approximately 36 and an on resistance of 336 ohms. This is the resistance of the channel. The source and drain parasitic resistances add 135 and 181 ohms respectively to the channel resistance to yield a total on resistance of 652 ohms.

The average off resistance of JFET devices is on the order of 10^9 ohms and is generally considered to be an open circuit (Ref 27:86). It will be considered to be open in this development.

When the JFET switch is in the "on" mode there is no bias applied, therefore, the device electrically looks like a diffused resistor and thus the JFET is nearly noiseless in passing the signal.

The gate current of the JFET in the "off" mode, I_{goff}, is important in that it determines the power consumption of the device. This current will be the reverse leakage current of the gate-channel p-n junction. The reverse leakage current value can be obtained from the literature (Ref 28:178) to be 10 nanoamps for a worst case approximation.

At 3 volts this yields a worst case power consumption of 30 nanowatts per multiplex switch.

Given the channel doping, channel length, and channel depth of this design, the switching time of the JFET's can be calculated to have a lower limit of 4 nanoseconds from the inequality

$$t_o > \frac{4kL^2}{eu_{ch}N_d d^2} \qquad \text{(Ref 28:255)} \qquad (4)$$

This value is more than adequate for this four by four electrode array. The switching time could become a critical parameter, however, in future designs containing hundreds of multiplexed electrodes.

In Figure 4-4 is a diagram of the JFET device structure arrived at through the preceding design development.

Electrical Characterization (Ref 29)

Figure 4-5 displays a functional equivalent circuit of one electrode and one column line leading to a source follower amplifier (not part of this design) showing the parasitic elements which the signal encounters. A description of the functional and parasitic components of the circuit follows.

C_e: metal-electrolyte interface electrical double layer capacitance.

R_e: metal-electrolyte interface resistance due to the exchange current.

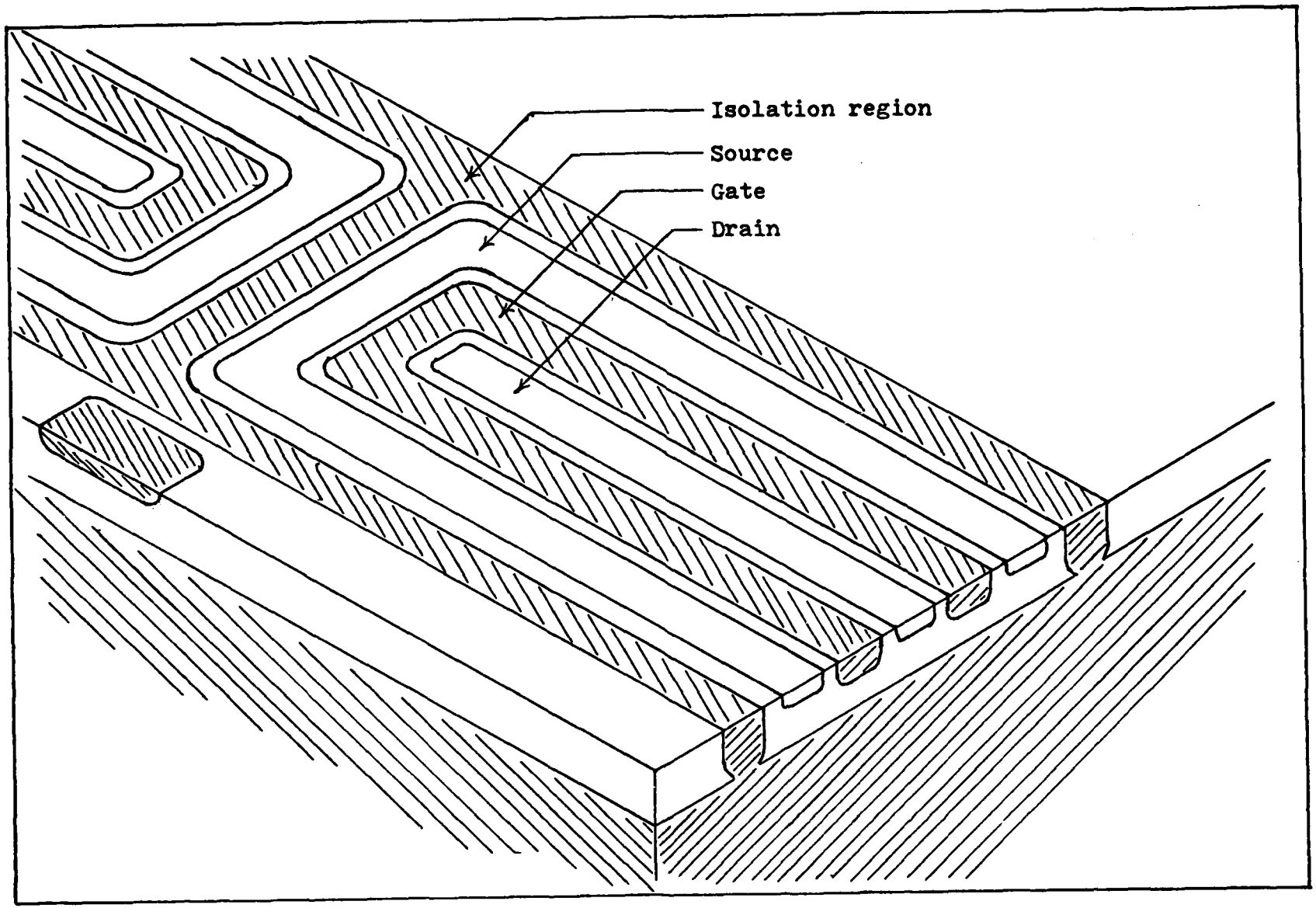

Fig. 4-4. Cross section of desired JFET structure.

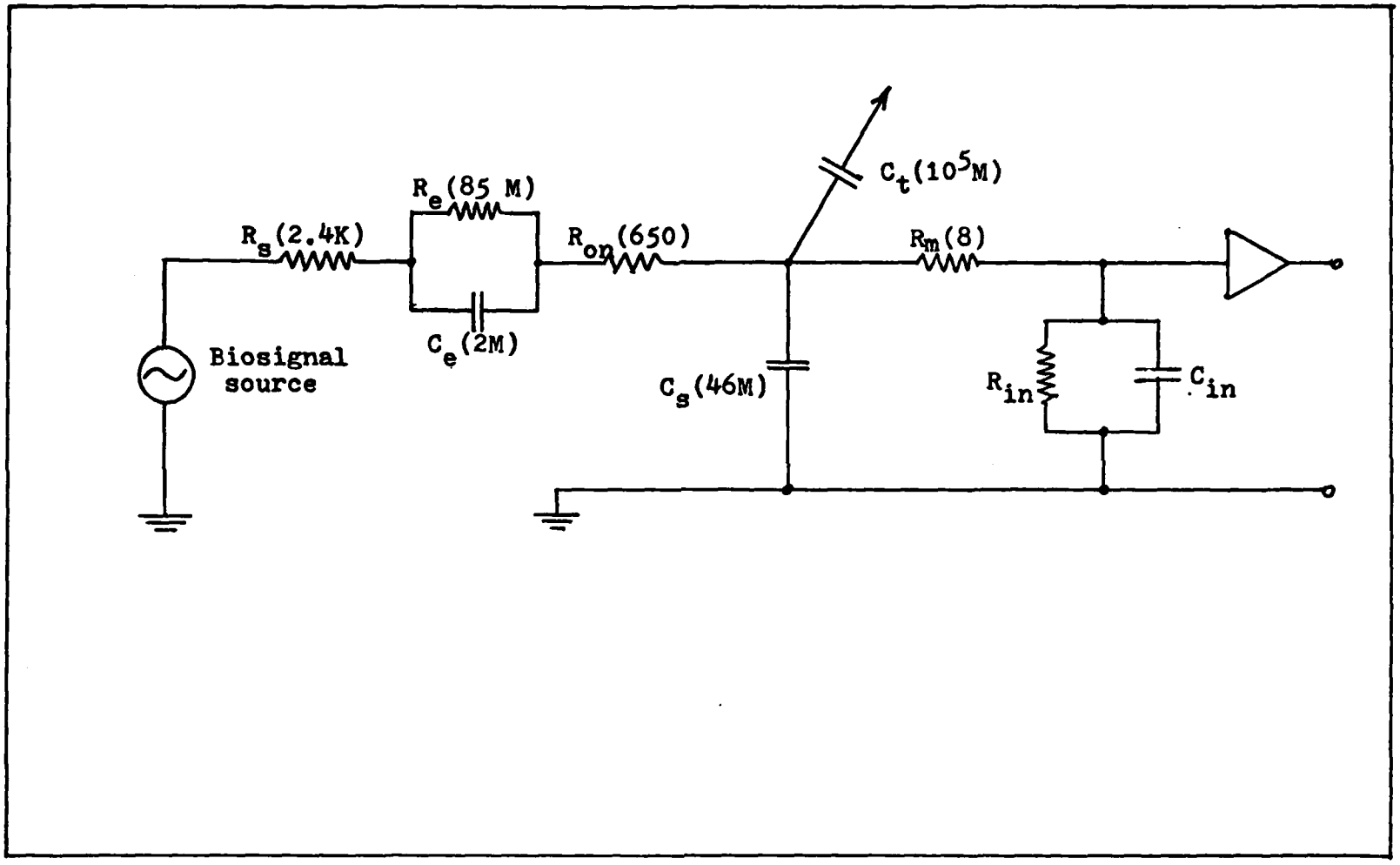

Fig. 4-5. Equivalent circuit of one electrode-column output lead of the microprobe (all impedance values in ohms, calculated at 30 Hertz)(Ref 31:201; 29:1066).

R_s: spreading resistance, resistance of saline bath of the CSF from the biological signal source to the electrode.

R_{on}: on resistance of the JFET multiplex switch.

R_m: resistance of the metallic leads from electrode to bonding pad.

C_s: total shunt capacitance to ground of device output lead.

C_{in}: input capacitance of the source-follower amplifier.

R_{in}: input resistance of the source-follower amplifier (C_{in} and R_{in} not part of electrode array device).

C_t: crosstalk coupling capacitance between output leads.

C_e, the capacitance of the Helmholtz electrical double layer of the metal-electrolyte interface, dominates the impedance, Z_e, of the electrode. This is desirable since this capacitive coupling prevents net charge transfer between the electrode and the tissue which in turn prevents tissue damage. In order to maximize the coupling, however, between the electrode and the signal generating tissue, it is desired to maximize the area of the electrode. Due to the highly local nature of C_e, the width of the dielectric of the Helmholtz capacitor is only 2 to 4 angstroms; roughening of the electrode surface through plating increases the capacitive area beyond its macroscopic dimensions and therefore improves coupling (Ref 22:242).

For this electrode design, each electrode has an exposed surface area of approximately 0.016 square millimeters which at a reported capacitance of the double layer of 0.2 picofarads

per micron squared (Ref 22:243), sets C_e of each electrode at 3100 picofarads. This yields an impedance at 10 Hertz of 5 megohms, which is acceptable when compared to the input impedance of the amplifier used with the device (100 megohms). It does, however, pose noise pickup problems unless an impedance buffer is placed close to the electrode to lower the impedance level.

R_e, the electrode resistance, is due to the exchange current across the Helmholtz layer of the metal-electrolyte interface, i_o. R_e must be minimized, which will minimize i_o, and thus minimize tissue damage as noted previously. For the gold electrodes of this device, R_e is calculated to be 85 megohms based on a reported R_e of 1.33×10^4 ohm-cm^2 (Ref 29:1068). This value changes for different metals and is largest for gold and platinum.

R_s, the spreading resistance, measures the resistance of the saline bath from the biological signal source to the recording electrode. Making worst case assumptions, the value of R_s in this device is calculated to be approximately 2.4 kilohms. This is insignificant compared to electrode impedance, Z_e.

R_{on} is the on resistance of the JFET multiplexing switch. In this device, R_{on} has a theoretical calculated value of approximately 650 ohms. Compared to the input impedance of the amplifier and the electrode impedance, R_{on} does not significantly effect the performance of the multielectrode probe, as assumed in the early stages of this design.

R_m is the worst case resistance of the longest gold lead; this has a value of approximately 8 ohms and is thus insignificant.

C_s, the total shunt capacitance to ground of the device, acts as a voltage divider with electrode capacitance, C_e, to attenuate the recorded signal. C_s includes the shunt capacitance of all leads to the substrate and of all leads to the extracellular fluid (treated as ground) and also the parasitic capacitance of the JFET devices. To minimize the parasitic effect of C_s, all lead widths should be kept to a minimum, and the two oxidation layers, between the leads and the substrate and between the leads and the CSF, should be kept uniform and as thick as feasible. For this device, the C_s of one electrode, JFET device, column lead signal path is 46 megohms at 30 Hertz. This is adequate compared to a C_e at 30 Hertz of 1 to 2 megohms.

R_{in}, the input resistance of the amplifier, acts with C_e of the electrode as a high-pass filter. Thus, R_{in} must be very large to prevent excessive attenuation of the recorded signal. To keep attenuation below 3 dB for the specific C_e of this device, R_{in} must be greater than or equal to 10^8 ohms.

C_{in}, the input capacitance of the amplifier to be used with our device, acts with C_e as a voltage divider to attenuate the recorded signal. The normal C_{in} of most input amplifiers of a few picofarads will be more than adequate.

C_t, the capacitive coupling between adjacent electrode leads, the crosstalk capacitance, also includes the capacitive coupling between the output leads and the electrodes they run alongside. Considering the worst case run between electrodes and leads of any output lead, C_t is calculated to be 0.1 picofarads. This translates to an impedance of over 10^5 megohms at 30 Hertz. This compares to a shunt impedance to ground of the same leads of 46 megohms at 30 Hertz. This high ratio of C_t to C_s removes nearly all coupling noise between output leads.

Referring back to Figure 4-5 and comparing the shunt and noise impedances, all measured at 30 Hertz (average frequency of cortical responses to visual data (Ref 30:329)), to the impedances in the line of the signal, also measured at 30 Hertz, it is observed that the recorded signal output by this multielectrode probe to the external input amplifier should be sufficiently undistorted to yield meaningful data.

In summary, the electrode array design problem is to design a multiplexed electrode array to simultaneously record the low frequency, microvolt signals across the cortical surface. The requirements of the electrode have been listed in detail and its design development described. Finally, the electrode device's electrical characteristics have been theoretically calculated. In the following section, the electrode array fabrication program will be discussed.

V. Electrode Fabrication

Introduction

A drawing of the final microprobe fabricated is shown in Figure 5-1 ready for lead attachment and final presurgical insulation. The four by four array of rectangles in the center of the square is the array of sixteen electrodes that will contact the cerebrospinal fluid (CSF) to record the cortico-electrical signals. They are approximately 120 by 80 microns on 250 micron centers. The dotted surface area indicates the chemical vapor deposition (CVD) silicon dioxide insulation. The large rectangular areas of exposed metal on the perimeter of the probe are the bonding pads. Wires leading to the external electronic monitoring equipment will be hand soldered to these. This is the reason for their large size. The exposed metal area extending along two sides of the central microelectrode array is the ground plane. The cortical signals will be measured relative to this ground. Due to the large bonding pads required for hand soldering and to practical handling purposes during surgical implantation, the probe is very large compared to the very small amount of chip area containing active devices. A secondary benefit of this large area is that the microprobe is easily extendable to several times the present number of electrodes in the array.

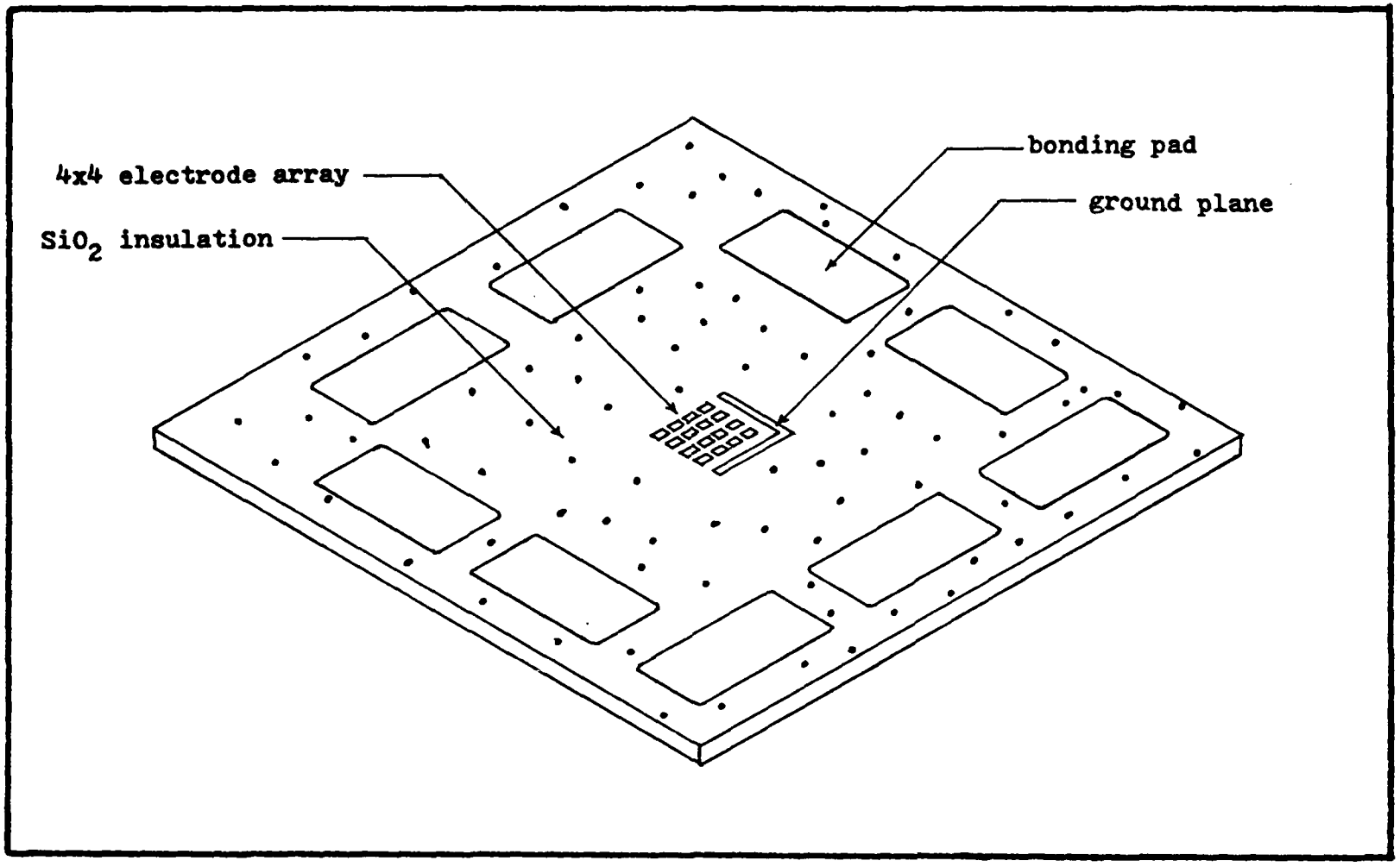

Fig. 5-1. The four by four multiplexed electrode array microprobe.

This section describes the fabrication process that results in the structure discussed above. The major steps in the process will be stated, followed by a more detailed description of the process. The original detailed process schedule is found in Appendix D. along with the revised process schedule arrived at through the initial fabrication run.

Fabrication Process

The major steps of the fabrication sequence are listed below.

1) Formation of the initial oxide layer on the substrate.

2) Three photolithographic masking and diffusion steps to construct the junction field-effect transistor (JFET) devices.

3) Formation of the final thermal oxide insulating layer over the probe surface.

4) Contact windows opened through the final thermal oxide layer.

5) Metallization and liftoff.

6) Overcoating with a CVD oxide insulation layer.

7) Exposure windows opened to the bonding pads and electrodes.

8) Lead attachment and final insulation.

The starting material is a p-type silicon substrate, 13 mils thick with a $\langle 100 \rangle$ orientation, with a 2 micron n-type epitaxial layer grown onto it. Substrate resistivity is 20 to 60 ohm-cm. Epitaxial wafers were chosen to simplify

the fabrication of the JFET devices. The n-type epitaxial layer provides n-channel JFET's which have a lower switch on resistance.

The major steps of the fabrication sequence are shown in Figure 5-2. Standard photoresist procedures are used throughout the diffusion steps to selectively etch windows through the silicon dioxide through which the dopants will diffuse. In this fashion, the geometries of the diffusions are controlled. These same photoresist-etching steps are used to define geometries in the contact windows, metallization, and exposure windows steps. For ease of fabrication and for yield considerations, 5 micron design rules have been used throughout the design of the device. This means no feature of the probe can be less than 5 microns wide and no two features can be closer together than 5 microns.

The first step of the fabrication sequence is to thermally grow 0.5 micron of silicon dioxide onto the surface in wet oxygen at 1050°C. This oxide is then selectively etched using photolithographic techniques with photoresist to open windows in the oxide over the areas where the dopant is to diffuse into the wafer. A p-type dopant, boron, is now diffused at 1100°C through the epitaxial layer to a depth of 3.5 microns, to join with the p-type substrate. This forms isolated pockets across the wafer. Each of these pockets will contain a single JFET device. Through these isolation regions, each JFET is electrically isolated by two back to back p-n junctions from the rest of the probe.

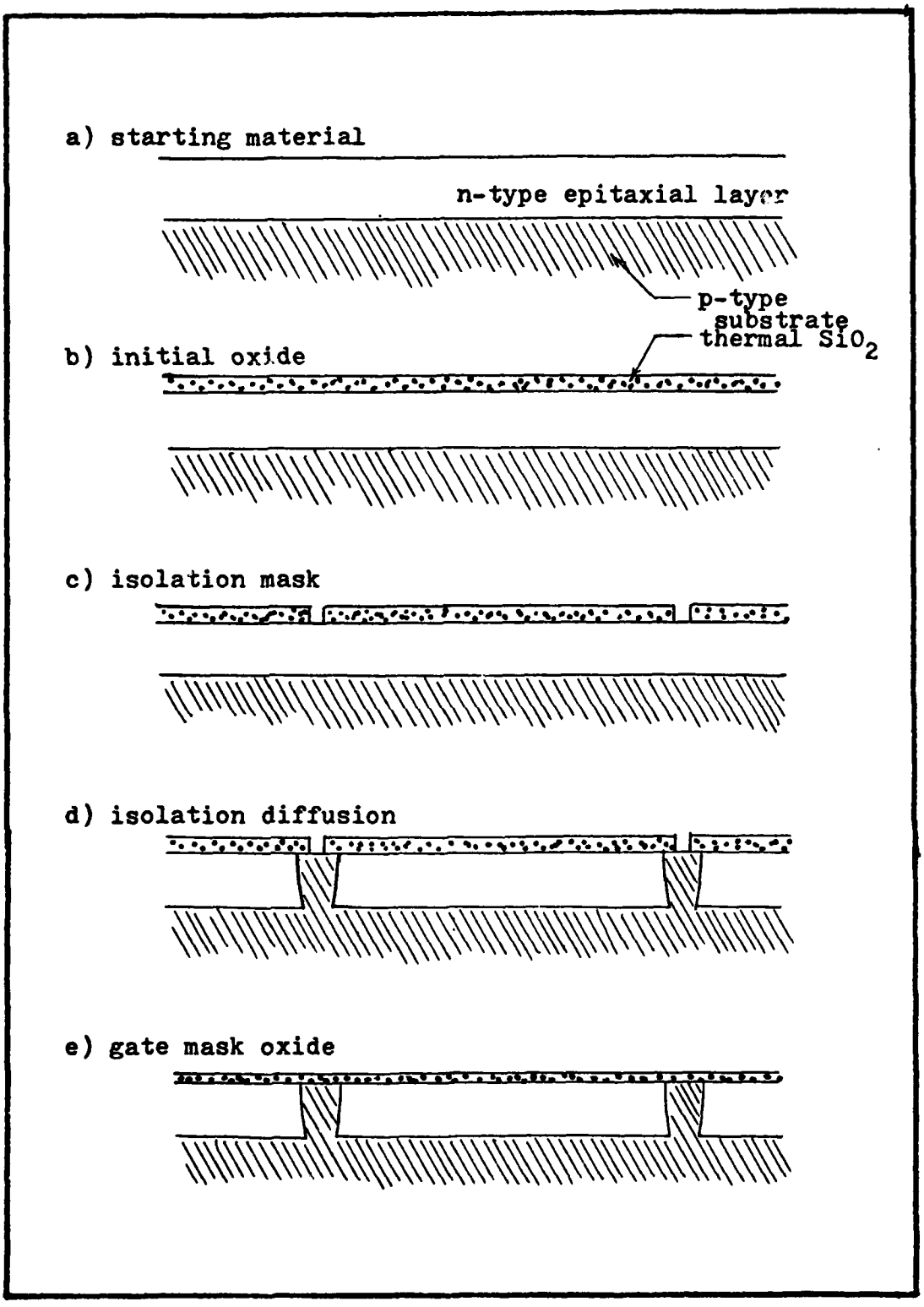

Fig. 5-2. The fabrication process sequence.

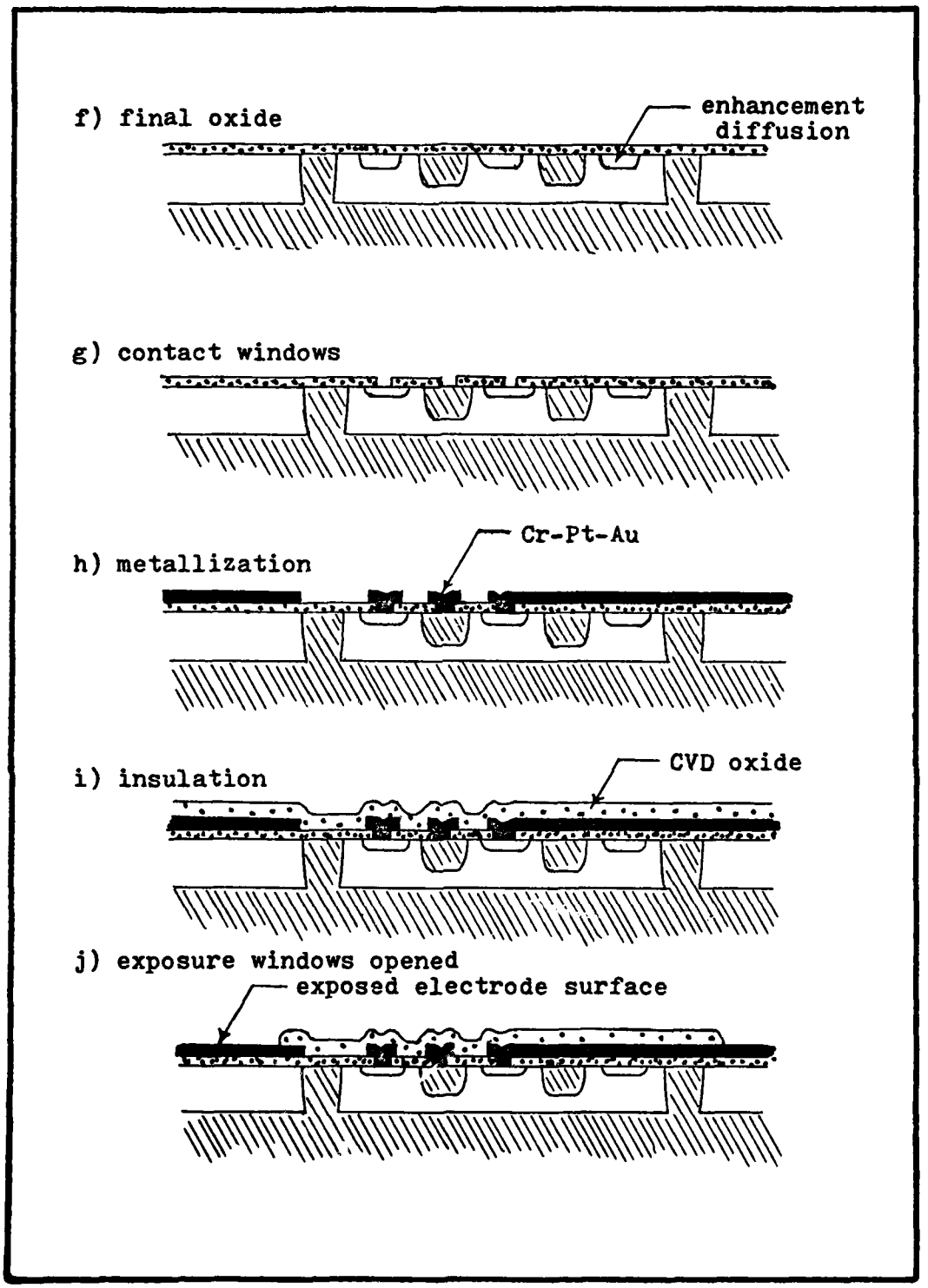

Fig. 5-2(continued).

Following the isolation diffusion, the remaining oxide layer is completely removed through another etching step and a new thermal oxide layer grown to 1400 angstroms to prepare the surface for the next diffusion, the gate diffusion.

The above steps result in the structure shown in Figure 5-2e. Steps c and d, shown in Figure 5-2 and discussed in the above paragraph, are now repeated for the gate diffusion and then for the enhancement diffusion. A final thermal oxide layer (1500 angstroms in wet oxygen) is grown to produce the JFET structure shown in Figure 5-2f.

The gate diffusion is another p-type, boron diffusion. It is diffused to a junction depth of 1.0 micron. The resulting n-type layer sandwiched between the p-type gate diffusion and the substrate forms the channel of the field-effect transistor. The gate diffusion also forms the 10 ohms per square crossover structures. The shallow n-type enhancement diffusion, using a $POCl_3$ source, increases the surface impurity concentration of the n-type source and drain regions to ensure ohmic contacts of the metal leads to these regions. Since the high surface impurity concentrations resulting from the isolation, gate, and enhancement diffusions do not degrade device performance, and are actually desirable in the enhancement and crossover regions, drive-in diffusions are not necessary in the fabrication of this probe.

The contact windows are next etched through the final silicon dioxide layer. These windows expose areas of the

source, drain, gate, and crossover regions to allow the metallic leads to make contact to these active regions.

A liftoff technique is used to define the device metal patterns. A negative photoresist is spun onto the wafer and the metal mask applied. The metal evaporation is then performed followed by the liftoff of the photoresist and the unwanted metal.

The metallization involves a three step, chromium, platinum, and gold, vacuum evaporation process. An initial base layer of 250 angstroms of chromium is first applied to the surface. The chromium acts as a "glue" as the gold does not adhere well to silicon or silicon dioxide. A layer of platinum, sandwiched between the chromium and the gold, prevents the gold from diffusing through the chromium to the silicon. This would defeat the adhesive effect of the chromium. A layer of gold, 2000 angstroms thick, is then vacuum evaporated onto the platinum. The liftoff is now performed by placing the wafer in an acetone solution. After this step, a cross section of one of the JFET-electrode cells is as shown in Figure 5-3.

The final silicon dioxide layer is now chemically deposited over the entire microprobe. This layer insulates the microprobe structure from the CSF. Windows are etched through the layer to expose the metal electrode sites, the ground plane, and the bonding pads. This results in the structure shown in Figure 5-1 and described in the introduction to this section.

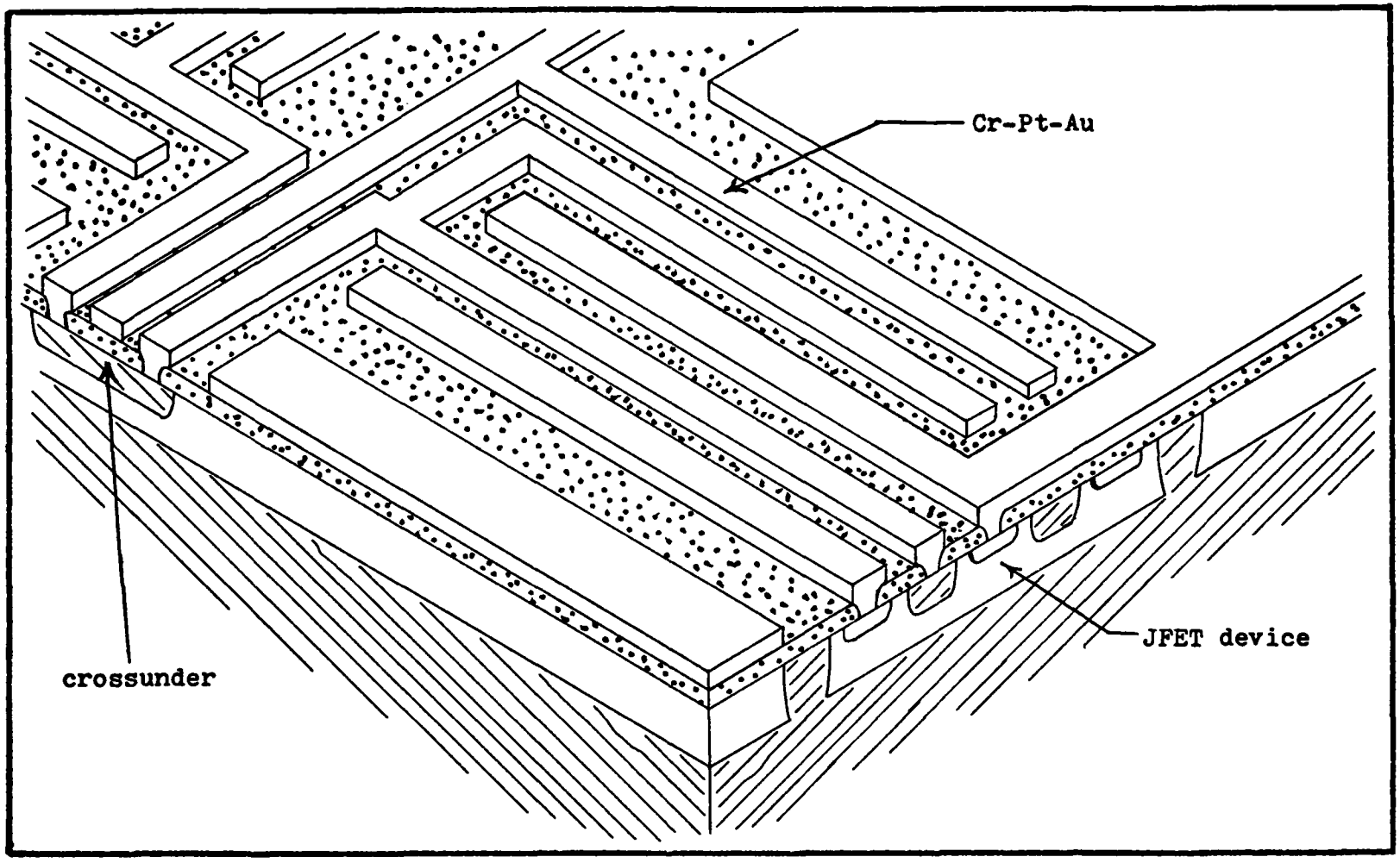

Fig. 5-3. Cross section of the JFET structure after metallization.

The lead wires, which will attach the microprobe to the electronic monitoring equipment, are hand soldered to the bonding pads. These bonds must be hand soldered to give the bonds and lead wires sufficient mechanical strength for handling during surgical implantation and testing. Thermocompression bonds would not provide this strength.

To insulate the bonding areas from the saline bath of the CSF, the entire structure, but for the center area containing the electrodes, is coated with moisture-proof epoxy and a final layer of medical grade Silastic for biocompatibility (Ref 8:478). This choice of insulation is one of many possible found in the literature (Ref 5:495-496; 7:218; 9). Further experimentation is needed in this area before a specific insulator is decided upon.

The process schedule described in this section was carried through a trial run. The results of this run, as well as the results from the system design exercise of Section III, will be stated and discussed in the following section.

VI. Results and Discussion

System Design

Results from the system design exercise will be discussed first in this section, followed by a discussion of the results from the electrode array design and fabrication process. In Section III of this thesis, a system to meet the requirements of the implantable electrode array recording and transmitting system of Section II was described. The following paragraphs discuss the capabilities and feasibility of that system. The system's data rate, power requirements, size, CMOS implementability, and long-term implantation possibilities are discussed.

Based on the assumptions and development of Section III, a data rate of one million six-bit words per second is obtainable. This data rate will allow an array of 10,000 electrodes, 100 rows by 100 columns, to be scanned at a frequency of 100 Hertz. The visual signals of the primary visual cortex are thought to have a frequency of approximately 20 to 40 Hertz (Ref 30). The Nyquist sampling rate for this information would then be about 80 Hertz. If it is assumed that no information of interest exists above 40 Hertz, the above stated system sampling frequency of 100 Hertz can be lowered to 80 Hertz. This would allow either a reduced data word rate, and thus ease speed requirements on system components, or else permit a larger array of electrodes.

From Appendix B, the power requirement of the implanted system is estimated to be approximately 6 milliwatts. Given examples from the literature (Ref 8; 17), this amount of power should be readily obtainable through a transcutaneous RF link. The 6 milliwatt value, however, could be increased by several milliwatts in order to increase the speed of the amplifier and comparator to obtain a megahertz data rate. An increase of this size should not be a problem as power levels as high as a kilowatt have been transmitted across the skin through RF links (Ref 32). However, there will still be a tradeoff between a desirable power level and an optimal data rate.

It is crudely estimated in Section III that the internal system, minus the transmitter and power circuitry, should cover no more than approximately a square centimeter, given a 100 by 100 array of electrodes on centers between 50 and 100 microns. This is small enough to prevent excessive flattening of the cortex by the flat integrated circuit electrode array. Based on examples from the literature (Ref 15; 17), the transmitter and power circuitry should fill a volume of no more than 28 millimeters by 28 millimeters by 2 millimeters. This is well within the system requirements.

Besides the transmitter and power circuitry, the electrode array and all internal system components should be implementable with complementary MOS (CMOS) technology. However, a combination bipolar and CMOS integrated circuit might yield

the most optimal speed to power ratio for the amplifier and the comparator (Ref 12).

A necessary requirement for the long-term implantation of this system is the transcutaneous transfer of information and power across the intact skin. This requirement should pose no problem for the system given the present level of technology in this field (Ref 15; 17). By using inert metals (gold or platinum) for electrodes, by only recording from and not stimulating the cortex, and by having the electrodes capacitively coupled to the tissue, the system should be able to be implanted for fairly long periods of time without excessive deterioration of the cortical tissue. However, preventing the degradation in performance of the electronics due to the CSF environment will be quite difficult, especially for the multiplexing gates of the electrode array. This insulation must not only provide protection for the transistor gates from the CSF, but also be capable of being selectively removed from the surface by photolithographic techniques in order that the electrodes (of microscopic dimensions) can be exposed to the bioelectrical signals of the cortex. This insulation will probably prove to be the limiting factor in the lifetime of the implantable system.

Electrode Design and Fabrication

The results of the design and fabrication of the prototype four by four multiplexed electrode array will now be discussed. First, the results of the design process will be considered in light of the design requirements. The results of an initial run through the fabrication process will then be discussed with the resulting modifications to the process schedule.

The calculation of the electrical parameters of the array device yields a shunt impedance to ground, Z_s, of 46 megohms at 30 Hertz. At the same frequency, impedance of the electode, Z_e, the series impedance seen by the recorded signal, is 1.7 megohms. This results in a favorable Z_s to Z_e ratio of 27.

Originally, to minimize R_{on}, the pinchoff voltage, V_p, of the JFET switches was chosen to be 3 volts. However, because R_{on} is in series with the megohm impedance of the electrode, its minimization is not essential. Therefore, V_p can be lowered to somewhere between one and three volts and an acceptable value of R_{on} still be obtained.

Because the JFET looks like a diffused resistor in the "on" mode, device noise is not a problem. Due to the shunt impedance to ground of the signal leads being several orders of magnitude lower than the impedance between the leads themselves, interlead coupling is not a problem. The shunt impedance of the signal leads to biological noise sources across the insulating boundary is greater than 46 megohms,

and so much greater than the series impedance along the signal path of 1.7 megohms (both impedance values calculated at 30 Hertz). Thus, biological noise should not present a problem.

The initial run through the electrode array fabrication process resulted in a nonfunctional device. The reasons were poor contacts, leakage paths between the drain, source, and gate, and cracking of the CVD silicon dioxide insulation layer.

The contacts between the metallization layer and the source, drain, and gate must be ohmic. The initial fabricated device's contacts were Schottky diodes with a forward voltage drop of approximately 2 volts. The existence of a Schottky diode implies that the enhancement diffusion in the source and drain areas was insufficient. This inference is supported by the fact that the sheet resistance of this diffusion measured hundreds of ohms/square rather than the desired 10 ohms/square. The insufficient enhancement diffusion is thought to have been caused by an unpredictable technical problem. The 2 volt forward voltage drop of the Schottky diodes is probably the result of incomplete opening of the silicon dioxide contact windows and a resulting thin layer of oxide between the metal leads and the source, drain, and gate. In future device process runs the opening of these windows should be carefully checked.

The leakage paths between the source, drain, and gate prevent the turning [illegible] JFET switch. They are most likely the result of impurities in the oxide insulation layer that separates the metallization from the substrate. To remove these impurities, and thus the leakage paths, more careful water cleaning procedures should be used, the oxide growth furnace tubes should be flushed with HCl immediately prior to use for critical oxide growths, and the entire fabrication process should be gone through without having to regrow any of the oxide masking layers. Also, a C-V measurement, to measure oxide impurity levels, should be taken of the oxide layers whose impurity content is critical.

The cracking of the CVD silicon dioxide over the large areas of gold is the result of the different contraction coefficients between the gold and the silicon dioxide during the cooling which follows the CVD process. This cracking can be stopped by adding a fraction of phosphorous (approximately 2 percent) to the CVD oxide during growth and by varying its thickness.

These results of the initial run through the process result in the modified process schedule found in Appendix D. This process schedule calls for more careful cleaning procedures, both an initial wafer clean and more complete rinsing steps. Also, an HCl flush of the oxide furnace tube just prior to the final oxidation step is included. Two

additional checks are called for in the modified schedule. These are a C-V measurement of the impurity content of the final oxide layer, and a check of the $POCl_3$ n-type source during the enhancement diffusion.

Anticipating that a functional device would be obtained through this thesis project, a bath test evaluation plan was drawn up to test and calibrate the electrode array device. Although not used, this plan is included as Appendix A in this paper.

The results of both the system design and the electrode array design and fabrication process have been stated. In the final section of this thesis, the conclusions drawn from these results will be stated and recommendations made for future studies.

VII. Conclusions and Recommendations

Conclusions

In order to test Kabrisky's theories of pattern recognition in the human visual system, a chronically implantable recording and transmitting system is required to simultaneously record the bioelectrical signals existing across the surface of the visual cortical areas and to transmit this data outside the body. It is feasible to build this system with present-day technology. It is feasible for the system to be built around an electrode array of 100 rows by 100 columns with electrodes on 50 micron centers, to have a system data rate of one million words per second, to have a power consumption of approximately 10 milliwatts at 3 volts, and to make the device long-term implantable in an animal subject with all transfer of information and power across the intact skin.

An essential component of this system is an integrated circuit multiplexed electrode array. A prototype multiplexed electrode array has been designed and fabricated as part of this thesis. The prototype device did not work due to technical problems encountered during the fabrication process. Therefore, the array design remains untested. It is clear, however, that standard integrated circuit technology is capable of producing a multiplexed electrode array device that meets the requirements set forth in Section IV of this thesis.

Recommendations

In pursuing the development of a four by four multiplexed electrode array microprobe suitable for gathering valid physiological data, the first step beyond this thesis should be to use the mask set and process schedule, generated by this thesis effort, to obtain an electrode array which meets the requirements for that array stated in Section IV. This device can then be used to gather physiological data in order to validate the use of the device design of this thesis in gathering meaningful data from the surface of the cerebral cortex.

If the device proves to yield useful physiological data, its performance over time in the CSF environment can be improved by modifying the gold metallization-CVD oxide insulator combination. A platinum-annealed silicon dioxide combination, or better yet, a platinum-silicon nitride metal-insulator combination, would significantly increase the protection of the device from the water and sodium ions of the CSF. A platinum-silicon nitride device should prove to be a valuable tool for gathering cortical data, be fairly inert in the CSF environment, and be extendable to larger arrays of electrodes.

Regarding development of a physiological data recording system capable of validating Kabrisky's pattern recognition theories, the first step is to obtain a working four by four multiplexed electrode array that can withstand several days of exposure to the CSF, probably a platinum-silicon nitride device. A concurrent step would be to breadboard the internal system and a simplified version of the external

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system. The internal system breadboard circuit should be designed and built to be implementable as an implantable monolithic integrated circuit. The platinum-silicon nitride device and these breadboarded circuits could then be used together to gather physiological data to both validate their design and to study various aspects of the nervous system. At this point it will probably be valuable to vary the size and resolution of the array to obtain specific requirements for these two parameters. Also at this point in the research program, it will be necessary to optimize the methods of protecting the device from the CSF environment.

The next step would be to build the internal system around a monolithic integrated circuit supporting both the electrode array and the associated internal circuits, minus the transmitter and power circuitry. This system would be capable of gathering very useful cortical data applicable to Kabrisky's pattern recognition theories.

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A. Evaluation Methods

In anticipation of obtaining a functioning microprobe device through this thesis project, a bath test evaluation plan was dr wn up. Though a functioning device was not produced and thus the evaluation plan not used, it is included here for possible use in future theses efforts.

Considering the use of the microprobe device to record extremely small, slow wave bioelectrical signals, 200-400 microvolts and 1-40 Hertz average, the microprobe must show a very high shunt impedance to the signal and a low electrode impedance at low frequencies relative to the shunt impedance. Also, the crosstalk capacitive coupling between output leads must be kept very low. Because of the CSF environment the device will be operating in, the change in device parameters with time submersed in a saline bath is very important. In light of these device requirements, the parameters to be evaluated are the electrode impedance, the recording bandwidth, the crosstalk capacitance, shunt capacitance to ground, the on resistance of the JFET multiplexing switches, and the encapsulation effectiveness. A proposed plan for the testing of these parameters will be covered in this appendix.

Electrode Impedance, Z_e. The electrode impedance, the impedance of the metal-electrolyte interface, is highly capacitive. It is important in that this is the impedance the microvolt slow wave signal must overcome to be recorded onto the microprobe. Because the biological signal is of

such low frequency, the capacitance of Z_e must be made relatively large to reduce Z_e to a workable level of a few megohms.

The test apparatus displayed in Fig. E-1 will be used to obtain values for Z_e as w ll as for the bankwidth and the crosstalk capacitance and will be modified to measure the shunt capacitance. The apparatus consists of an oscillator signal source which produces a sinusoidal signal of 100 millivolts amplitude. This voltage is divided by the 1000 megohm resistor and the electrode impedance, Z_e. The resistance of the isotonic saline bath is negligble compared to Z_e. By amplifying and measuring the signal across Z_e, the value of Z_e can be calculated by the voltage divider equation. This apparatus is a modified version of that found in Robinson (Ref 17:1070)

Bandwidth, BW. Because we are cnly interested in the slow wave potentials of the cortex and not the faster action potentials, the bandwidth required is very narrow but very low frequency, 1-40 Hertz. It is desired to have a nearly constant Z_e across this narrow bandwidth for accurate measurements. The Z_e testing apparatus will be used to test the bandwidth by varying the frequency of the source and observing the change in signal attenuation on the oscilloscope.

Crosstalk Capacitance, C_t. Because of the grounded substrate and the low impedance between the leads, the crosstalk on any output lead should be nil. The test apparatus of Figure E-1 is again used, but in this test, there are two signal leads to the submersed electrode. The lead from the

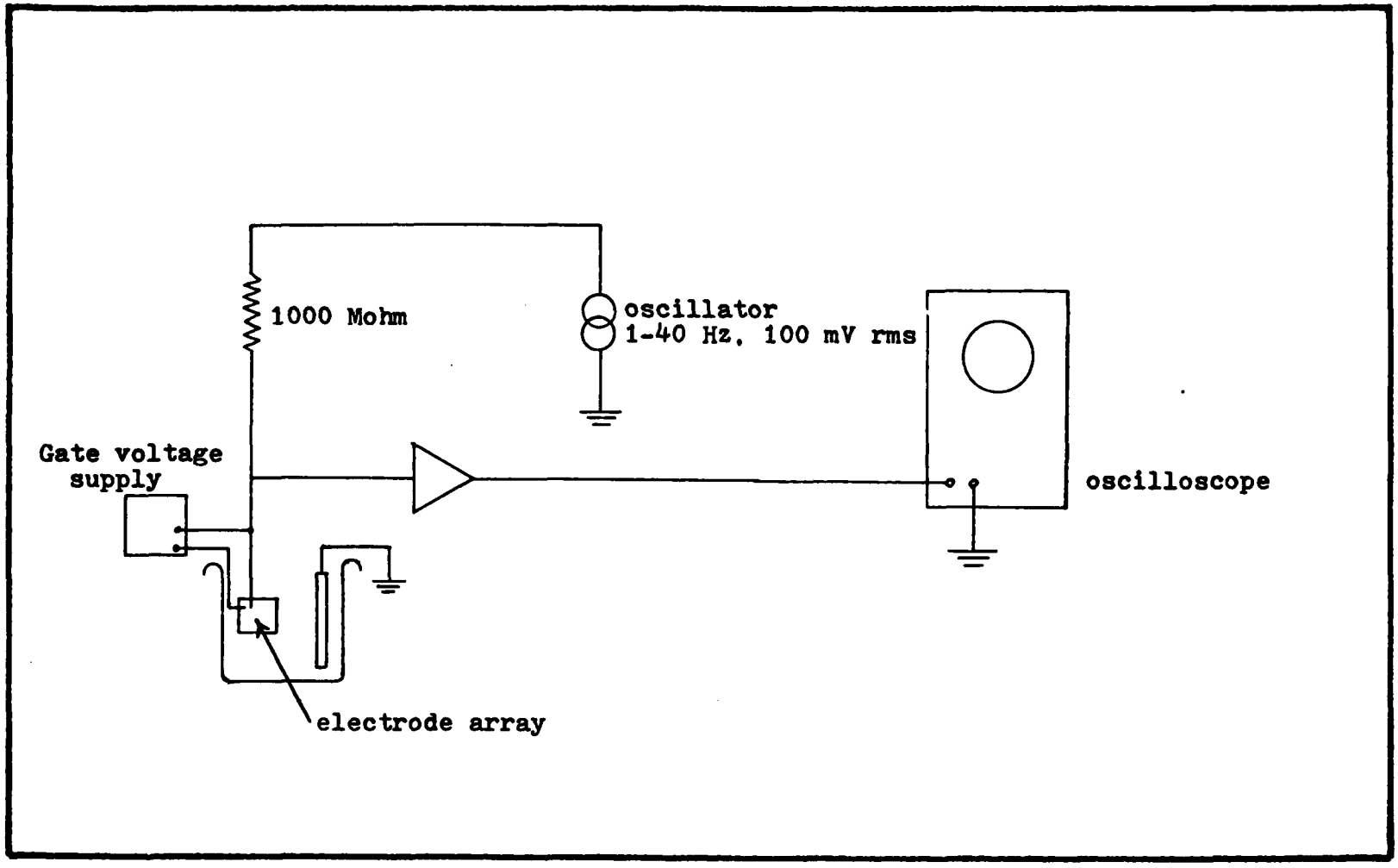

Fig. E-1. Electrode array testing and calibration apparatus (Ref 29:1070).

signal source is hooked up as in the figure, but in this test, the output is measured across an electrode lead adjacent to the signal lead. The frequency of the signal source is changed from 1-40 Hertz while the cross coupled signal is measured across the adjacent lead.

Shunt Capacitance, C_s. As explained earlier, the shunt capacitance must be kept to a minimum, hopefully an order of magnitude less than the capacitive portion of Z_e, as the two act as a voltage divider to attenuate the signal.

The apparatus of Figure E-1 is again used, but in this test the output is measured from an output lead to the grounded substrate. The electrode need not be submersed into the saline bath in this case and the substrate is grounded.

On Resistance, R_{on}. The on and off resistances of the JFET switches determine the resistance to the signal offered by the switch in the on position and the effectiveness of the switch in blocking the signal in the off position, respectively. These values are measured using an integrated circuits laboratory probing apparatus to apply contacts directly to the leads contacting the source, drain, and gate regions of the JFET's and measure the devices' electrical characteristics.

Encapsulation. Due to the degrading effect of the CSF on the performance parameters of implanted electronics, the encapsulation problem is very important. In this microprobe, the only insulation protecting the active area of the device is one micron of CVD silicon dioxide. Though this should be adequate to give constant device parameters over a few hours

in the CSF, the required time for the short-term implant experiments of this stage of the research program, much development will have to be done in this area in future devices.

To test the degradation of the parameters of the device, the parameters measured above are compared to the same parameters measured after submersing the device in an isotonic saline bath for various periods of time.

B. Internal System Power Estimate

In this appendix, the estimated power consumption of the implanted system described in Section III is computed. The power consumption of each element of the system is estimated from the power requirements of currently available integrated circuits in the commercial market. Then, the total power requirements of the implanted system is computed by summing the values for these elements. For this appendix, a system containing an electrode array of 100 rows by 100 columns will be assumed. A supply voltage of 3 volts will also be assumed. The estimate of the total power consumption obtained in this manner is admittedly a crude approximation, but should be valuable in evaluating the feasibility of implanting the said system and providing power through an RF link across the intact scalp.

The electrode drive circuit is actually a 100-bit shift register. Based on the power requirements of an eight-bit parallel output CMOS shift register (National MM54C164) (Ref 21), the estimated power requirements of the drive circuit is less than 1 microwatt.

Each column of the multiplexed electrode array is a 100 into 1 multiplexer. There are 100 columns, and so 100 of these multiplexers. From the power consumption of an 8 into 1 CMOS multiplexer (National CD4051)(Ref 21), the power requirements of the electrode array is estimated to be less than 1250 microwatts.

The power requirements of the 100 source followers is computed to be very much less than 1 microwatt based on previously built devices from the literature (Ref 7:217).

The multiplexer block includes a 101-bit shift register and 100 into 1 multiplexing gate. The power consumption of the shift register is the same as for the drive circuit, less than 1 microwatt. The multiplexing gate power requirement is 0.01 times the electrode array requirement and so is less than 13 microwatts.

A bipolar micropower operational amplifier has been designed (Ref 13) that consumes less than 850 microwatts. It is assumed that this amplifier can be integrated into the otherwise CMOS circuitry as is done in BiMOS integrated circuits (Ref 12).

The pulse modulator consists of a monostable multivibrator, a comparator, and a current source. A CMOS multivibrator is available (National MM54C221)(Ref 21) that consumes less than 1 milliwatt at the estimated firing rate of this system. The comparator is assumed to have the same power requirements as the operational amplifier of the previous paragraph, 850 microwatts. The power consumption of the current source will depend upon the system data rate and the size of the associated capacitor. For a megahertz data word rate and a 100 picofarad capacitor, the current source will consume about 1 milliwatt of power.

The power consumption of the carrier modulator is determined to be 250 microwatts from a transmitter designed and built by Ko (Ref 15:355)

Summing the values for all the elements of the implanted system, its estimated power requirement is less than 6 milliwatts. Based on implanted RF link power supplies from the literature (Ref 17), this power requirement is readily obtainable.

C. JFET Design Development

In Section IV, the design development of the junction field-effect transistor (JFET) multiplexing switch, was briefly discussed. In this appendix the details of that design development are discussed. The various device parameters will be determined beginning with the channel thickness and pinchoff voltage, then the gate width and gate length, the doping of the gate and the channel, and ending with the on resistance of the JFET device. The design objectives of the device were to minimize the on resistance and limit the pinchoff voltage to 3 volts for biocompatibility considerations. Throughout the development refer to Figure 4-1 in Section IV.

From Burger and Donovan (Ref 26:271)

$$V_p = \frac{a^2 e}{2k} N_d (1 + \frac{Nd}{Na})$$

where

V_p = pinchoff voltage
a = channel depth = d
e = unit electron charge
k = dielectric constant for silicon
N_d = channel doping
N_a = gate doping (upper gate)

In this case, the lower gate is more lightly doped than the channel and is grounded. It is thus out of the circuit and so for this situation a = d (normally 2a = d). Also, in this case N_d is very much less than N_a. This reduces equation (1) to

$$V_p = \frac{d^2 e}{2k} N_d. \qquad (2)$$

For reasons to be shown, this can be rearranged to

$$\frac{1}{deN_d} = \frac{d}{2kV_p} \qquad (3)$$

Now, as for the on resistance of the channel,

$$R_{on} = \rho_{ch} \frac{L}{Zd} \qquad (4)$$

where ρ_{ch} is the resistivity in the channel, and substituting

$$R_{on} = \frac{1}{e\mu_{ch}N_d} \frac{L}{Zd}$$

where μ_{ch} is the electron mobility in the channel, and rearranging

$$R_{on} = \frac{1}{deN_d} \frac{L}{\mu_{ch}Z}$$

Substituting from equation (3)

$$R_{on} = \frac{d}{2kV_p} \frac{L}{\mu_{ch}Z}$$

$$R_{on} = \frac{d}{V_p} \frac{1}{2k\mu_{ch}} \frac{L}{Z} \qquad (5)$$

As mentioned above, V_p must be less than or equal to 3 volts. Due to fabrication considerations, d must be greater than or equal to 1 micron. In this range of V_p and d, μ_{ch} remains nearly constant. Therefore, to minimize R_{on}, d/V_p should be minimized, and so V_p is chosen to be 3 volts and d is chosen to be 1 micron.

Also, to minimize R_{on}, the Z over L ratio must be maximized. Due to the 5 micron rules used in the design of the device, the smallest L obtainable is 15 microns.

To maintain a simple JFET structure, and taking full advantage of the 250 micron device centers, the maximum Z is found to be 580 microns. These values yield a Z to L ratio of approximately 39.

To determine the doping profile of the device, we write equation (2) as

$$N_d = \frac{2kV_p}{d^2e}$$

which yields $N_d = 4 \times 10^{15}$ cm^{-3} for this case and a corresponding channel resistivity of 1.3 ohm-cm.

The only requirement on the gate doping, N_a, is that it be much greater than the channel doping N_d. Due to fabrication considerations, N_a will be approximately 5×10^{20} cm^{-3}.

This doping profile and device structure results in

$$R_{on} = \rho_{ch} \frac{L}{Zd} = 336 \text{ ohms.}$$

Adding to this value the parasitic drain and source resistances, the total on resistance of the JFET device is found to be 650 ohms.

In summary, the preceding design development results in the following JFET parameters:

Pinchoff voltage:	3 volts
On resistance:	650 ohms
Channel length:	15 microns
Channel width:	580 microns
Channel depth:	1 micron
Channel doping:	4×10^{15} cm^{-3}
Gate doping:	5×10^{20} cm^{-3}

D. Processing Schedules

Introduction

The following is the detailed process schedule by which the electrode array microprobe prototype, discussed in Sections IV and V of this thesis, was fabricated. Following this will be the revised process schedule arrived at through the work of this thesis.

Original Process Schedule

1. Starting material: substrate: p-type, (100), 20-40 ohm-cm
   epitaxial layer: n-type, 0.91 ohm-cm

2. Initial oxidation:

   a. Standard clean CL1.
   b. Oxidation: 1050°C; schedule--10 min dry O_2, 40 min pyrolytic steam, 10 min anneal in N_2.
   c. Nominal thickness: 0.5 micron

3. Mask: apply mask 1 (isolation diffusion); back side protection unnecessary.

4. Isolation diffusion:

   a. Standard clean CL1.
   b. Diffusion: 1100°C; $Boron^+$ "b" sources; schedule--120 min in 1 liter/min N_2 + 30 cc/min O_2.
   c. Strip all SiO_2 in conc. HF.
   d. Standard clean CL1.
   e. Oxidation: 1000°C; schedule--5 min dry O_2, 10 min steam, 5 min N_2.
   f. Nominal parameters: x_j = 3.5 microns, SiO_2 = 1400 angstroms.

5. Mask: apply mask 2 (gate diffusion); back side protection unnecessary.

6. Gate diffusion:

   a. Standard clean CL1.
   b. Diffusion: 1050°C; Boron+ "b" sources; schedule--30 min in 1 liter/min N_2 + 30 cc/min O_2.
   c. Strip all SiO_2 in conc HF.
   d. Standard clean CL1.
   e. Oxidation: 950°C; schedule--5 min dry O_2, 20 min steam, 5 min N_2.
   f. Nominal parameters: x_j = 1.0 micron, SiO_2 = 1500 angstroms.

7. Mask: apply mask 3 (enhancement diffusion); back side protection unnecessary.

8. Enhancement diffusion:

   a. Standard clean CL1.
   b. Diffusion: 1000°C; $POCl_3$ sources; schedule--5 min soak, 10 min diffuse (dopant light on), 5 min purge (all three steps: 70 cc/min N_2 source, 500 cc/min N_2 bypass, 150 cc/min O_2).
   c. Nominal parameters: R_s^2 = 10 ohms/square; x_j^2 = 0.4 micron.

9. Final oxidation:

   a. Strip all SiO_2 in conc HF.
   b. Standard clean CL1.
   c. Oxidation: 950°C; schedule--hand push (1 min), 5 min dry O_2, 12 min steam, 5 min N_2, hand pull (1 min).
   d. Nominal thickness: 1000 angstroms.

10. Mask: apply mask 4 (contacts); back side protection unnecessary.

11. Mask: apply mask 5 (metal liftoff); back side protection unnecessary.

12. Metallization:

   a. Standard clean CL3.
   b. Evaporate 250 angstroms Cr, 750 angstroms Pt, 2000 angstroms gold.
   c. Perform liftoff.

13. Insulating oxidation:

   a. CVD oxidation
   b. Nominal thickness: 1 micron.

14. Mask: apply mask 6 (exposure windows); protect back side.

15. Packaging: Hand solder wires to bonding pads.

Revised Process Schedule

1. Starting material: substrate: p-type, (100), 20-60 ohm-cm
   epitaxial layer: n-type, 0.91 ohm-cm

2. Initial clean: schedule--10 min soak in TCE, 10 min soak in acetone, 10 min soak in methanol, DIW rinse (10 min above 14 megohms).

3. Initial oxidation:

   a. Standard clean CL1.
   b. Oxidation: 1050°C; schedule--10 min dry O_2, 60 min pyrolytic steam, 10 min anneal in N_2.
   c. Nominal thickness: 5000 ang

4. Mask: apply mask 1 (isolation diffusion); back side protection unnecessary.

5. Isolation diffusion:

   a. Standard clean CL3.
   b. Diffusion: 1100°C; $Boron^+$ "b" sources; schedule--110 min in 1 liter/min N_2 + 30 cc/min O_2, 10 min in 500 cc/min O_2.
   c. Strip all SiO_2 in 10:1 DIW:HF.
   d. Standard clean CL3.
   e. Oxidation: 1000°C; schedule--5 min dry O_2, 10 min pyrolytic steam, 5 min N_2.
   f. Nominal parameters: x_j = 3.5 microns, SiO_2 = 1400 ang

6. Mask: apply mask 2 (gate diffusion); back side protection unnecessary.

7. Gate diffusion:

   a. Standard clean CL3.
   b. Diffusion: 1050°C; $Boron^+$ "b" sources; schedule--25 min in 1 liter/ min N_2 + 30 cc/min O_2, 5 min in 500 cc/min O_2.
   c. Strip all SiO_2 in 10:1 DIW:HF.
   d. Standard clean CL3.

e. Oxidation: 950°C; schedule--5 min dry O_2, 25 min pyrolytic steam, 5 min N_2.
f. Nominal parameters: x_j = .9 micron, SiO_2 = 1500 ang

8. Mask: apply mask 3 (enhancement diffusion); back side protection unnecessary.

9. Enhancement diffusion:

a. Standard clean CL3.
b. Diffusion: 1000°C; $POCl_3$ source; schedule--5 min soak, 10 min diffusion (dopant light on and check for source bubbling), 5 min purge. For soak, diffusion, and purge: N_2 source 70 cc/min, N_2 bypass 500 cc/min, O_2 150 cc/min.
c. Nominal parameters: R_s = 10 ohms/square; x_j = 0.4 micron.

10. Final oxidation

a. HCl flush of oxide tube (overnight or about 8 hours).
b. Strip all SiO_2 in 10:1 DIW:HF.
c. Strandard clean CL3.
d. Oxidation: 950°C; schedule--5 min dry O_2, 25 min steam, 5 min N_2.
e. C-V measurement of oxide impurity content.
f. Nominal parameters: SiO_2 = 2000 ang, final x_j(gate) = 1.0 micron, adequate C-V measure to be determined.

11. Mask: apply mask 4 (contacts); back side protection unnecessary.

12. Mask: apply mask 5 (metal liftoff); back side protection unnecessary.

13. Metallization:

a. Evaporate 500 ang Cr + 700 ang Pt + 2000 ang Au.
b. Liftoff.
c. Alloy 500°C for 5 min.

14. Insulating oxidation:

a. CVD oxidation (Add approximately 2 percent phosphorous).
b. Nominal thickness: 1 micron.

15. Mask: apply mask 6 (exposure windows); protect back side

16. Packaging: Hand solder wires to bonding pads.

Standard Procedures

The CL1 and CL3 cleaning procedures listed below have been slightly revised due to the results of the prototype process run of this thesis.

CL1:

3:2, H_2SO_4:H_2O_2 (self heating)	15 min
DIW rinse	10 min above 14 M -cm
10:1, DIW:HF	15 sec
DIW rinse	10 min above 14 M -cm
Spin dry	2 min

CL3:

Same as CL1 except 100:1, DIW:HF for 20 sec

PR1: all mask steps except for liftoff

1) 2 hour bake, 220C, N_2 flow
2) Waycoat (-), spin on at 4000 rpm
3) Prebake, 70C, 20 min, N_2 flow
4) Exposure appr 4 sec, 0.6 mW/cm^2
5) Develop, butyl acetate, then xylene
6) Postbake at 150C, 30 min, N_2 flow
7) etch in buffered HF:NH_4F, 1:6
8) photoresist strip (O_2 plasma), 10 min

PR2: for liftoff mask

1) 2 hour bake, 220C, N_2 flow
2) KTI + 2, 30 cs, spin on at 3000 rpm
3) Prebake at 90C, 30 min, N_2 flow
4) Exposure, 10 sec, 0.6 mW/cm^2
5) Develop, KTI developer:DIW, 1:1
6) Postbake at 90C, 30 min, N_2 flow
7) Liftoff, boiling acetone 55C

VITA

Joseph Allen Tatman was born on 12 November 1955 in Indianapolis, Indiana. He graduated from Ben Davis High School in Indianapolis in 1974 and continued his education at the University of Notre Dame in South Bend, Indiana on an ROTC scholarship. He received a Bachelor of Science degree in Electrical Engineering from the Notre Dame College of Engineering in 1978. Through the ROTC program he was commissioned into the USAF upon graduation. He entered the Air Force Institute of Technology, School of Engineering, as his first assignment in June 1978. He can be located at:

2 East Main Street, Apartment 3
Fairborn, Ohio 45324

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Bioelectrode array, microelectrode, multiplexed electrode array, implantable electronics, microprobe, multielectrode probe, biomedical integrated circuits.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The pattern recognition research effort being conducted at the AFIT Bioengineering Laboratory motivated the design of an electrode array microprobe capable of simultaneously recording the bioelectrical signals existing over a large surface area of the cortex of the mammalian brain. Data recorded from this device should increase the present level of knowledge of the interconnections of the various areas of the cerebral cortex and thus be instrumental in the development of theories on the pattern recognition capabilities of the

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human brain. An implanted system has been designed around this microprobe to detect the cortico-electrical signals, multiplex and modulate these data, and then transmit them across the intact scalp to external recording equipment. The electrode array microprobe, itself, makes use of junction field-effect transistors integrated directly onto the array substrate in order to multiplex the probe's output leads. The first example of a four by four version of the electrode array has been fabricated. It did not function as designed because of technical problems and a revised process schedule was produced.